JFSA

Journal of Futuristic Sciences and Applications
Vol. 3(2), Jul-Dec 2020, pp. 64-72
doi: 10.51976/jfsa.322007
www.gla.ac.in/journals/jfsa
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Memory Architecture: Low-Power Single-Bit Cache

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ABSTRACT

Researchers investigated the functionality and efficiency of the single-bit cache memory architecture in terms of numbers. There are three different memory locations in a single-bit cache. A write driver, an SRAM cell, and a sensing amplifier are a few of these parts. SRAM blocks and sensing amplifiers are extensively used in constructing single-bit cache memory to reduce power usage. Both process corner simulation and circuit Monte Carlo simulation have researched their potential applications. It was subsequently determined that a forced stack design was more energy-efficient than a single-bit cache architecture.

Keywords: *Write Driver Circuit (WDC); Sense Amplifier (SA); Single Bit SRAM VMSA Architecture (SBSVMSA); Static Random-Access Memory (SRAM); Voltage Mode Sense Amplifier (VMSA).*

1.0 Introduction

Low-power memory architecture is gaining popularity as more battery-powered commercial solutions are released. The number of transistors has increased due to leakage current, resulting in an SRAM block that consumes much power even when it is not in use. Consider how much power and space it will require when creating the memory [1-3]. Memory design must be adaptable enough to accommodate modifications to logical patterns by allowing changes in the overall amount of memory available. This ensures the SRAM design process is sound by incorporating the test results into the suggested SRAM architecture for CMOS technology ranging from 90nm to 45nm.

1.1 Power reduction techniques

It is unnecessary to sacrifice a circuit's speed, usability, or any other characteristic to lower its power consumption.

1.1.1 Sleep transistor technique

State-destructive techniques damage PMOS or NMOS transistors irrevocably when their supply voltage or ground is connected to a sleep transistor. Transistors are made worthless in this fashion. Other names for the two techniques include VDD and gated-GND. Figure 1(a) shows how the sleep semiconductor technology breaks the link between the logical network's operation and the sleep transistors' activity.

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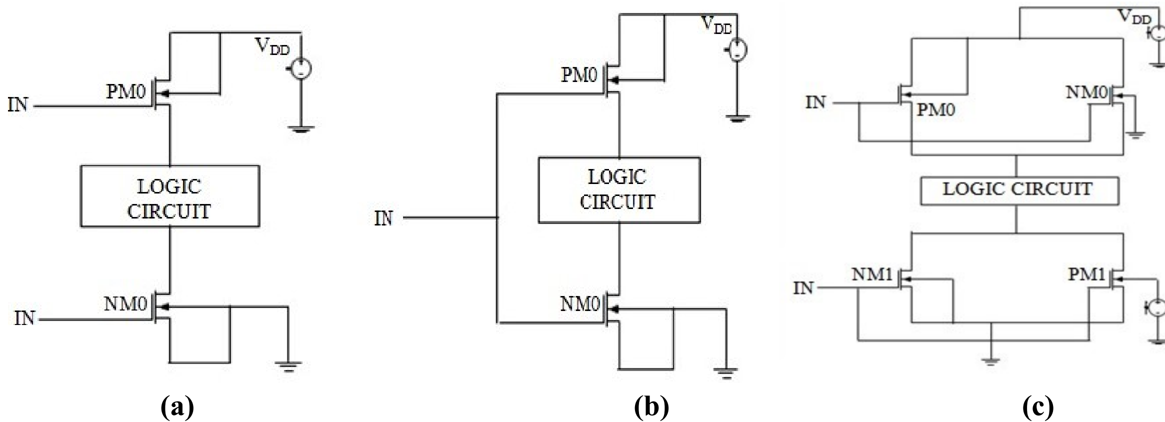
1.1.2 Forced stack technique

Figure 1 (b) depicts an illustration of a forced stack. Increasing the number of transistors in a circuit is another way to save electricity. [4] Stacking transistors lower leakage current to below the threshold when two or more transistors are turned off at once.

Figure 1: a) Sleep Transistor Technique, b) Forced Stack Technique, c) Dual Sleep Technique



(a) **(b)** **(c)**

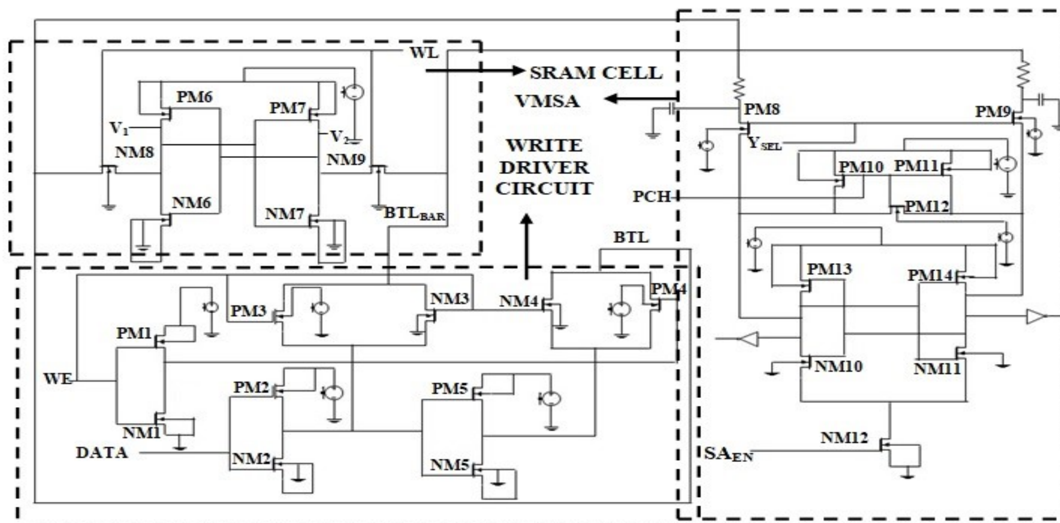
1.1.3 Dual sleep technique

In this process, two NMOS transistors and two PMOS transistors are employed. On the other hand, the header and footer employ NMOS and PMOS transistors. Both the on and off states of the transistor are switched on. Figure 1(c) [5-9] illustrates standby mode using NMOS and PMOS.

2.0 Single-Bit Memory Architecture

Figures 2 and 3 use the WDC, SRAMC, VMSA, and VLSA blocks to build a single-bit cache memory [10-13]. The following are the three parts of the description: Bit and we are two of the pins that plug into the WDC. BL and BLBAR are two of the pins that exit the WDC. The VMSA accepts the following five inputs: Ysel, BL, BLBAR, PCH, and SAEN. The word line (WL) and voltage inputs V1 and V2 are among the input pins on the SRAMC (V3 and V4).

Figure 2: Schematic of Single Bit Cache Memory Architecture having VMSA



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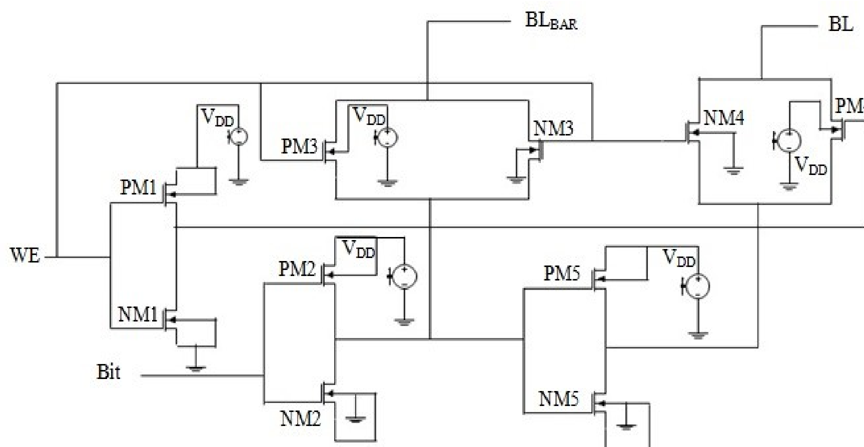
2.1 WDC

Before or while using the word lines of the chosen cell, the write driver must quickly relocate the bit lines underneath the write margin cells. Two common categories of data storage devices are shown in Figure 3. The moment someone starts to type, the WE indication starts to flash. If this isn't the case, the printed driver lines and the data lines can be separated without using a WE. Because fewer transistors worry about, the discharge is quick and straightforward. The write driver is advised for most write operations if layout restrictions can be removed and configuration is simple. By changing the number of transistors in a column, users can change the original design in addition to passing transistors and inverters for CMOS and NMOS [14].

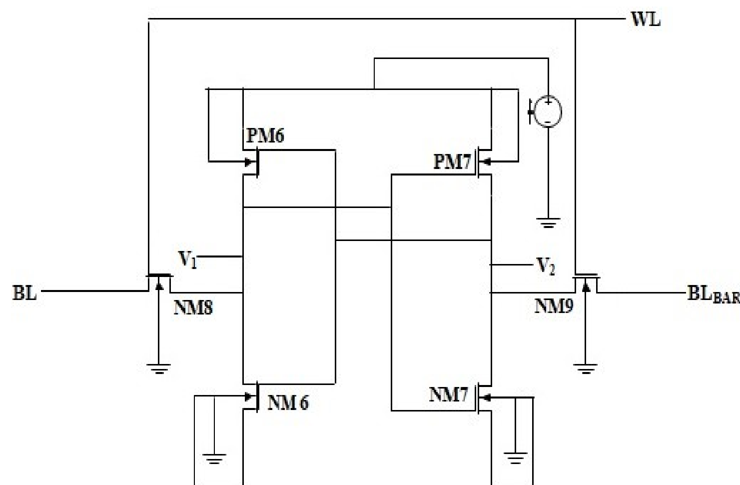
Figure 3: WDC Schematic



2.2 Conventional SRAM

Low-voltage and low-power applications make use of it. Each Bit is held in place by a circuit that has a latching capability. Figure 4 depicts PM6 and PM7 pull-up PMOS transistors driving NMOS transistors NM6 and NM7 [15]. The BL and BLB lines connected to the NM8 and NM9 pass transistors allow for data reading and writing. Bit lines increase the noise tolerance.

Figure 4: SRAM Cell Schematic



It is possible to calculate the value of voltage swings using differential circuits. DRAM cells never need to be updated since they always have logic 0 or 1 stored inside them [16]. The transistor size has a significant impact on the SRAM architecture. Since NMOS conducts almost twice as much as PMOS, inverters must have an NMOS width of 0.09um. If the logic in these devices is to be changed, the gate transistors must be at least three times larger than the NMOS inverter transistors. They shouldn't, however, get too big as it would take up more space in the room.

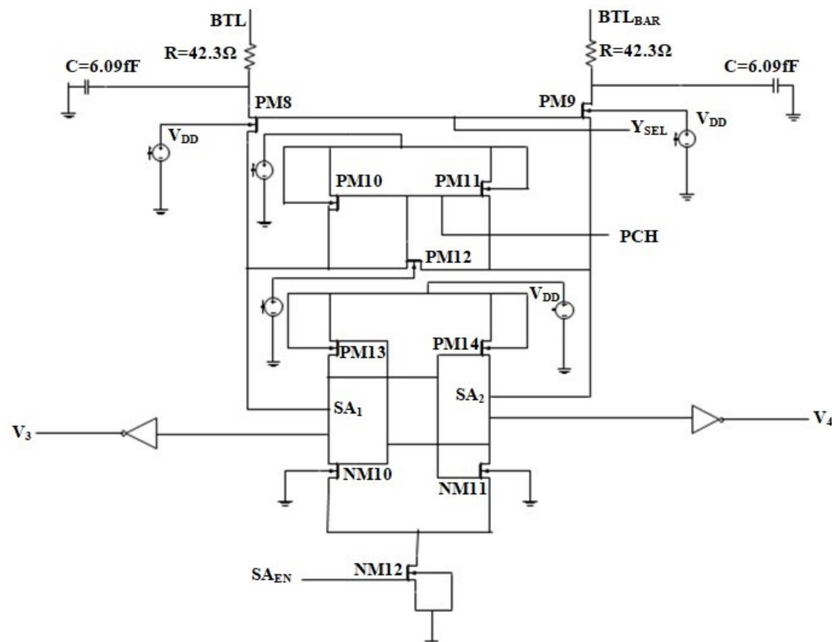
2.3 Sense amplifier

The sensing amplifier raises the analog voltage differential during bit line reading. Digital productions that have been amplified have a single point of departure and a huge range of motion. An SRAM cell can be smaller since the driving transistors don't have to drain the bit lines completely [17,18]. The read activities cause the cell to sluggishly the most. Longer bit lines necessitate additional transistors, which increases capacitance. In this case, care must be used when deciding on the load capacitor and the sensing amplifiers' timing. The SAen signal can be used for this.

2.3.1 Voltage mode sense amplifier

The MOS differential voltage sense amplifier circuit already uses the simplest differential sensing type. A differential amplifier can only have one small-signal output if it functions properly.

Figure 5: VMSA Schematic



The ability of a differential amplifier to boost actual signal differences while suppressing background noise determines how effectively it performs. For these and other reasons, a basic differential voltage amplifier is not used in memories, as shown in Figures 5 [19, 20].

3.0 Analysis of Result

The outputs of the circuits have been shown and described in this section. To determine how resistance (R) affects how much power a circuit consumes, the total power consumed by single-bit cache memory is compared to variations in R's value.

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Figure 6: O/P of WDC

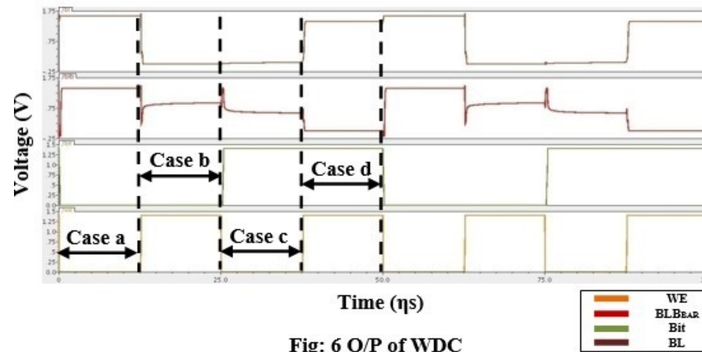


Fig: 6 O/P of WDC

Figure 6 depicts the wave's form following the WDC's activation. Criteria are satisfied if and only if the following circumstances exist: Wire = 0; Bit = 0; and BLBAR = direct voltage. Only three other regions, WL, BL, and BLBAR, are devoid of voltages. This indicates that the voltage of the Bit is virtually equal to VDD because it is identical to VDD in voltage.

Figure 7: O/P of SRAM Cell

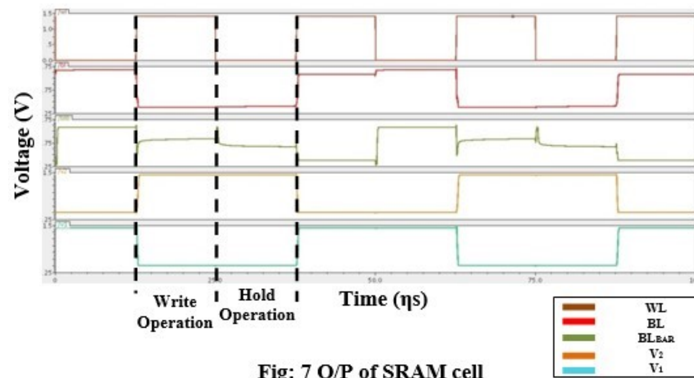


Fig: 7 O/P of SRAM cell

An SRAM cell used in a "write-and-hold" application is shown in Figure 7. Data can be stored and retrieved using a sensing amplifier's NM6, PM6, and NM6 access transistors (NM8 and NM9).

Figure 8: O/P of VMSA

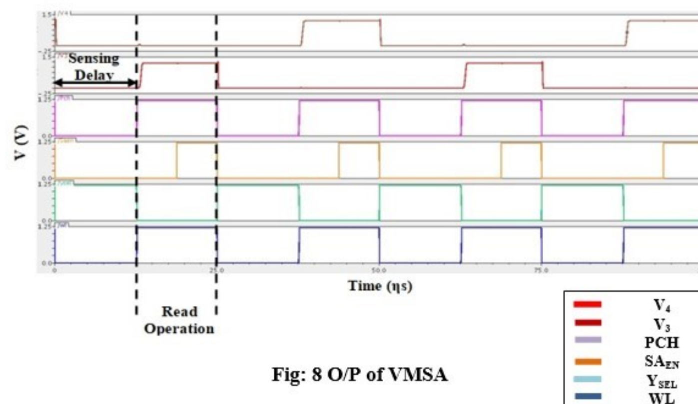


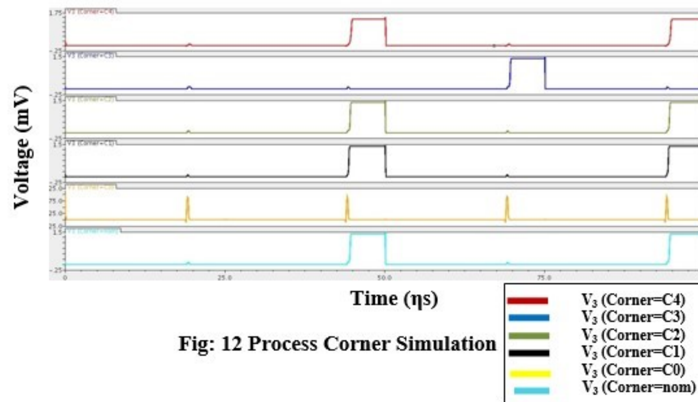
Fig: 8 O/P of VMSA

Figure 8 displays the VMSA data reading when both SAEN and WL are high. Only the sense amplifier can currently read data from the bit lines of the SRAM cell. Then, data is sent to V3 and V4 using bit lines.

The "six corners" simulation in particular

a) Because it is SS in V3 (Corner=C4), both NMOS and PMOS are slow.
b) Because V3 (Corner=C3) is SF, PMOS is quicker than NMOS.
c) Because in V3 (Corner=C2), NMOS and PMOS are moving at the same speed.
d) PMOS is slow, and NMOS is fast since V3 (Corner = C1) is FS.
e) NMOS and PMOS are exceptionally quick because V3 is FF.
f) Both the NMOS and PMOS are developed in V3 (Corner=nom).

Figure 9: Process Corner Simulation



Since the FF in corner V3 (Corner=C0) is both NMOS and PMOS fast, Figure:9 shows this circuit is inappropriate. The Monte Carlo simulation was used to evaluate the stability of the circuit for the VTH SAEN. The results of the simulation are shown in

Figure 10: Monte Carlo Simulation

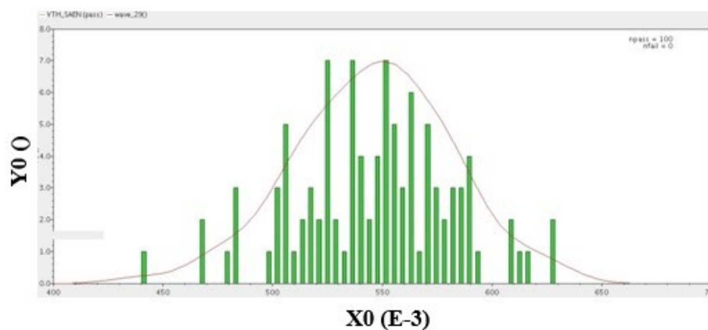


Table: 1 SBSVMSA Different Parameter

S.No.	Parameters	Power Consumption	No. of Transistors	Sensing Delay
1.	R=42.3Ω	15.21 µW	32	23.42ηs
2.	R=42.3KΩ	12.52µW	32	23.42ηs

Resistance cuts down on power use because it stops the current flow in a circuit. Tables 1 and 2 show that it does not affect area, performance, or speed.

Table: 2 Different SBSVMSA Parameters When Using Various Power-Reduction Techniques Over VMSA

S.No.	Architecture / Techniques	SBSVMSA		
		Power Consumption	No. of Transistor	Sensing Delay
3.	Dual Sleep Technqiue	13.12 µW	36	22.75 ηs
1.	Sleep Transistor Technqiue	13.33 µW	34	22.25 ηs
2.	Forced Stack Technqiue	13.33 µW	34	22.75 ηs

Table 3: SRAM with VMSA Power Consumption While Using Various Power-Reduction Techniques

S.No.	Architecture / Techniques	SBSVMSA		
		Power Consumption	No. of Transistor	Sensing Delay
3.	Dual Sleep Technqiue	10.13 µW	36	22.45 ηs
1.	Sleep Transistor Technqiue	9.18 µW	34	22.78 ηs
2.	Forced Stack Technqiue	9.108 µW	34	22.85 ηs

Table 3 illustrates the trade-off between space and power use: as power use declines, space increases. The power reduction strategy was used to lower transistors instead of the VMSA dual sleep methodology (in terms of transistors).

4.0 Conclusion

Using SRAM and Sense Amplifier blocks of single-bit cache memory for power-saving purposes, a low-power architecture employs the dual sleep approach, the sleep transistor technique, and the footer stack technique. Both process corner simulation and circuit Monte Carlo have undergone accuracy evaluations.

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