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Using Power Reduction Techniques, a Comparison of Differential and Latch Type Sense Amplifier Circuits

Dharmendra Kumar Tiwari, Narendra Kumar Verma** and Jitendra Singh Kirar****

ABSTRACT

Researchers have investigated several different sense amplifiers' yield and other quantitative features. Amplification is required for various power-saving methods, including the sleep transistor, the sleep stack, the sleepy keeper, and others. This study aims to evaluate how much energy is consumed by the many different sense amplifier topologies. Simulations have shown that adopting a sleep transistor approach can significantly reduce the amount of power lost even while operating at 1.2V.

Keywords: *SRAMC (Static Random-Access Memory Cell); VMDSA (voltage mode differential sense amplifier); Sense Amplifier (SA); VLSA (voltage latch sense amplifier); CLSA (current latch sense amplifier).*

1.0 Introduction

The development of smaller transistors has led to increased VLSI density and efficiency of devices [1]. Wires are used to link the transistors that make up an integrated circuit. Time and power are exchanged between semiconductors over worldwide networks. Many VLSI applications, such as the buses that link cache memory to CPUs, rely on global communication latency as VLSI technology develops to submicron scales. This is because submicron sizes are required for VLSI technology. [2] With more time passing, the four-way latency of this worldwide semiconductor connectivity will get worse. More than one type of signal transmission may be utilized thanks to several transceivers, which connect the various channels via which signals can be conveyed. As the use of battery-powered computers becomes more widespread, new low-energy storage options are being developed. Because of the leakage current, the number of transistors in the SRAMC system has risen, turning it into a block that requires a lot of power. SRAM blocks have a huge impact on the architecture of modern SoCs and how they are designed.

Utilizing sensing amplifiers, data is often accessible from static random-access memory cells (SRAMC) and dynamic random-access memory (DRAM) (DRAM). Data of high quality may tolerate many different types of noise while still faithfully portraying the information in a memory cell. They find that even moderate levels of noise are intolerable at times. Several circuits require

**Corresponding author; PhD Scholar, Department of Mechanical Engineering, United University, Prayagraj, Mathura, Uttar Pradesh, India (E-mail: dharmu.tiwari@gmail.com)*
***Madhav Institute of Technology & Science, Gwalior, Madhya Pradesh, India (Email: narendra.verma@itmgoi.in)*
****Department of Mechanical Engineering, RGPV (Rajiv Gandhi Prodyogiki Vishwavidyalaya, State Technical University), Bhopal, Madhya Pradesh, India*

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quick sensing amplifiers to cut down on the amount of time spent waiting. There is a significant amount of memory that makes use of bit lines. Interconnection is becoming an increasingly essential factor in developing sub-micrometer CMOS devices to reduce the amount of delay that occurs on-chip. Possibly, high-speed sensing amplifiers are required for large-chip high-speed signal repeaters [3-5]. The market for battery-powered mobile devices and embedded systems is expanding, and this growth is occurring concurrently with the expansion of the VLSI (large-scale integrated circuit) sector. Cache memory information can take up as much as sixty to seventy percent of the chip's surface area. When additional chips are used, the speed of the CPU slows down [6-8]. Businesses are looking at the possibility of developing a low-speed, low-power memory circuit to keep up with the ever-increasing expansion of VLSI systems. Individual chip failure rates are affected by adding or removing one million transistors at a time. The sensory amplifier is the main topic of this article (SA). It is now the case that high-performance microprocessors employ more than half of their transistors for cache memory, and it is anticipated that this percentage will continue to rise in the future [9–12]. Because the SRAMC in these chips operates effectively even when significant external sounds are present, the built-in stock is usually utilized. Consequently, more people started investing in developing computers that consume less power. If the device has the appropriate SRAMCs, it can store the memory it requires. A city can progress rapidly if it is well planned and efficiently managed. Memory blocks of the SRAMC wouldn't exist if it weren't for the SA, which can detect high frequencies. The configuration of the sensing amplifier determines the amount of time and energy required to access the memory. Memory devices' peripheral circuitry largely relies on SA for their operation. [13-16] Power-operated SA can decrease the gap between memory cells and the arbitrary logic levels of Boolean circuits by converting signals from bits to digital logical levels. This is accomplished by converting the signals. Memory loss and the amount of time it takes to recover are significantly influenced by the rate at which these structures expand. For CMOS memory to compete with conventional integrated circuits, it must expand faster, be more robust, and consume less power. The SA memory will not be useful to us in achieving these objectives. A common occurrence is an increase in the amount of parasite space used by the bit line concurrently with the expansion of the total memory capacity of the system. This bit line has been expanding [17–20] as the use of memory that requires a lot of energy has gotten increasingly widespread.

2.0 Power Reduction Techniques

This section discusses low power reduction strategies used in amplifiers such as the VMDSA, CMDSA, CLSA, and CLSA.

2.1 Sleep transistor technique

For this treatment, most people employ sleep transistors [21]. Figure 1 shows that the pull-up network is connected to both the VDD and the GND.

2.2 Sleepy-keeper technique

A mattress that can be folded into a bed by stringing together PMOS transistors in series between the pull-up network and VDD and the pull-down network and GND, this technique employs NMOS and PMOS transistors builds a circuit. This method makes it simpler to control outflow wells without modifying the operation of a small field circuit. While the device is in sleep mode, an

NMOS transistor connected to VDD and a pull-up network is activated. This guarantees that the value of the data is always "1." A PMOS transistor is wired with both the pull-down network and GND. Doing this maintains the data's value of "0". As seen in Figure. 2 [22], a "0" data value is maintained by turning on a second PMOS transistor.

Figure 1: Circuit Diagram of Sleep Transistor Technique

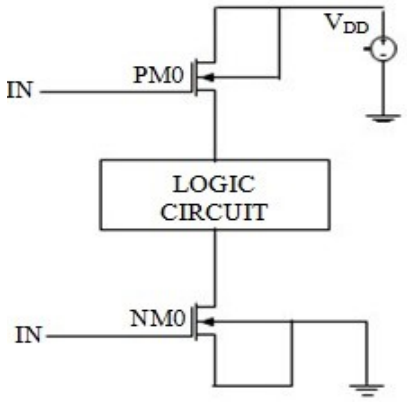
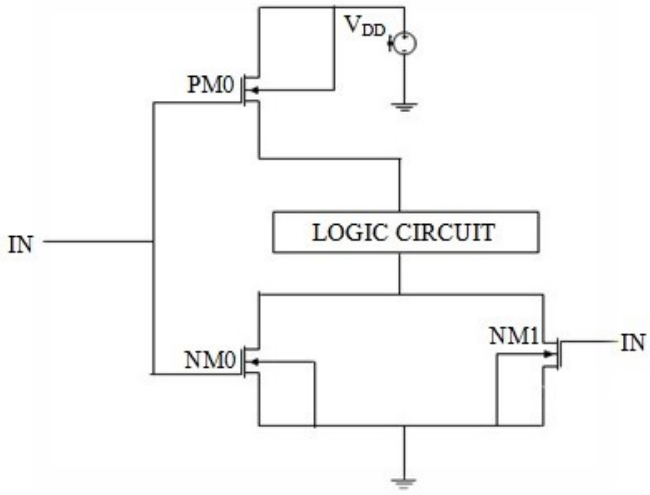


Figure 2: Circuit Diagram of Sleepy Keeper Technique



3.0 Sense Amplifiers

The sensing amplifier is a crucial element in terms of memory. Sense amplifiers (SAs) have developed into a distinct class of semiconductor memory circuits due to their quick evolution [23-27]. Since sensing does not damage the circuits, it is not necessary to feed the circuits with new data after sensing. Sensory amplifiers must almost always fulfill the following requirements:

3.1 Differential type sense amplifier

The circuit for the MOS sense amplifier has every element needed for differential sensing. Background noise can be reduced while real-world signal discrepancies can be increased. Since amplification uses so much energy and goes slowly, it cannot serve as a memory [28].

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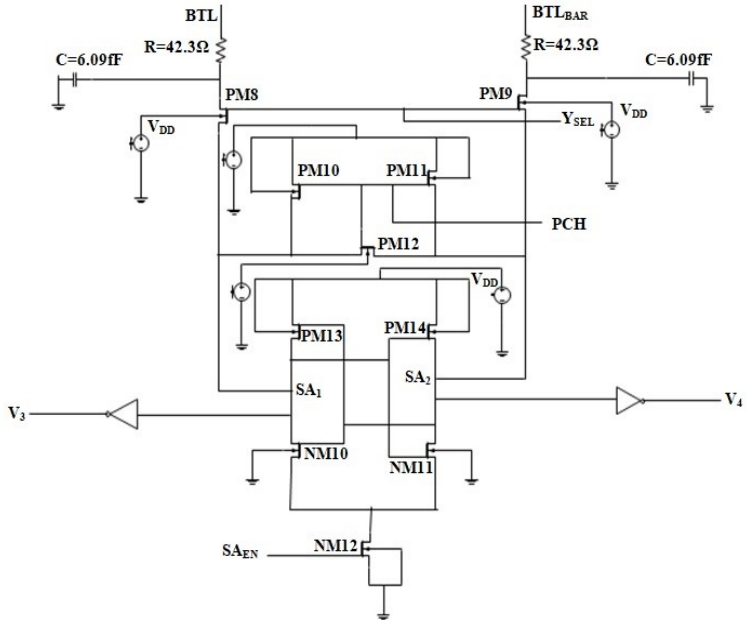
3.1.1 Voltage mode differential sense amplifier

A short MOS differential voltage sense amplifier circuit with all the elements needed for differential sensing is shown in Figure 3.

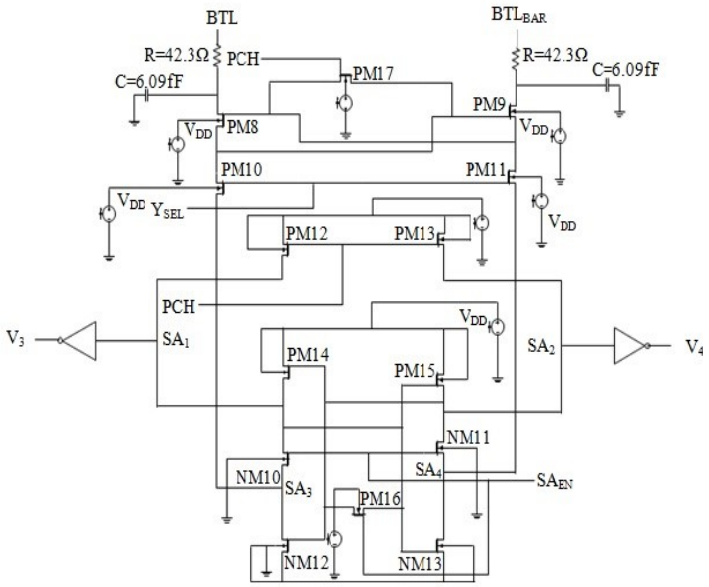
Figure 3: Schematic of Voltage Mode Differential Sense Amplifier



A differential amplifier's output must only have one end. The value of a differential amplifier depends on its capacity to amplify the difference between two real signals while ignoring background noise. Simple differential voltage amplification is not used in memory due to its slow working speed, high power consumption, and the large offset [29, 30].

3.1.2 Current mode differential sense amplifier

Figure 4: Schematic of Current Mode Differential Sense Amplifier



Differential current detection is used to find the difference between the input and output of the current-carrying amplifier. The anticipated use of the CMDSA is shown in Figure 4. Four Pmos transistors are used to enhance the signal (PM8-PM9-PM10-PM11). When utilizing a Pmos, similar latching and delay timings are applied to internal nodes SA1 and SA2 [31-34].

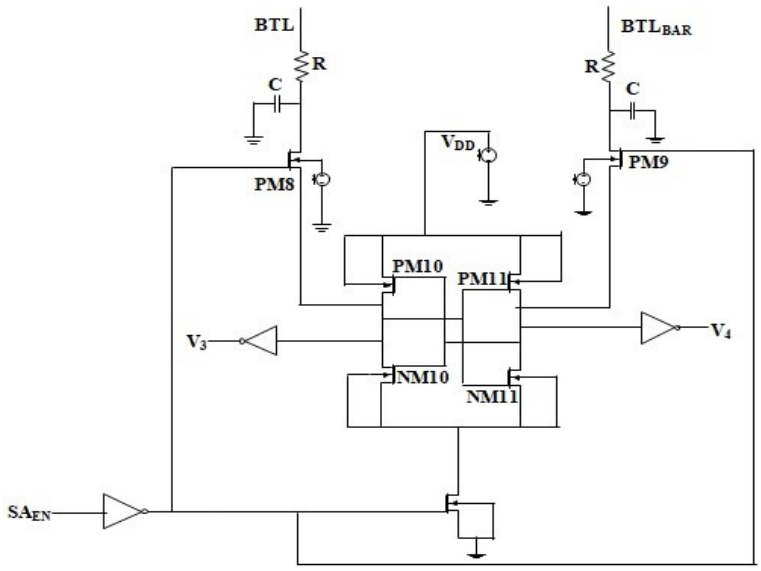
3.2 Latch type sense amplifier

Two inverters are used in the six-transistor SRAMC architecture to provide a sensing amplifier. The latch-type SA is preloaded and positioned in the high-gain metastable zone to start sensing [35]. If the latch-type SA is too close to the bit-lines, a "0" bit-line will be left empty; as a result, the latch-type SA must be kept away from the bit-lines.

3.2.1 Voltage latch sense amplifier

Figure 5 shows the designs for the voltage latching sensing amplifiers. The nodes in this system are pre-charged using bit-lines. Bit lines are immediately moved to internal nodes of a circuit being built [36-38].

Figure 5: Schematic of Voltage Latch Sense Amplifier



The PM8 and PM9 pass transistors turn on as soon as the WL is raised. The permissible internal nodes of a sensing amplifier increase with the distance between two-bit lines. Every time the inverters PM10, NM10, PM11, and NM11 send the sensor signal SAen, the differential voltage grows until it reaches its maximum swing output.

3.2.2 Current latch sense amplifier

The SA is a circuit that creates cache memory. The voltage supply to each bit remains constant throughout the reading, even when one-bit line drains and the other. There is a sign of a current lock on the amplifier in Figure 6.

The discharge delay is caused by the large bit-line capacitance and the small access transistor. In this stage, SA transforms an analog signal into a digital signal [39,40]. The bit lines' voltage differential is sent into the CLSA's SA3 and SA4 inputs. The SA1 and SA2 outputs will

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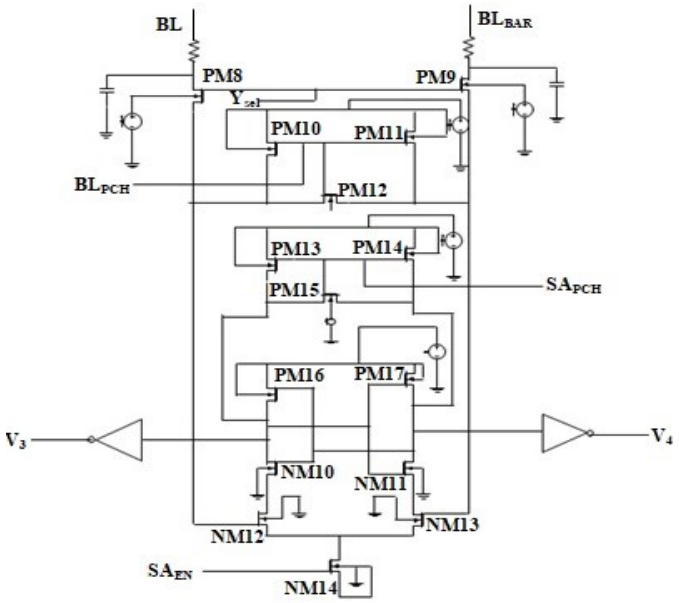
discharge if the SAEN pull-up resistor is cranked high. NM12 can receive more current because it has higher Vgs than NM13. Because of this, V3 uses up its energy reserves faster than V4.

Figure 6: Schematic of Current Latch Sense Amplifier



4.0 Comparison Table

The power requirements of several sense amplifiers are covered in this article, both with and without power-saving techniques.

Table 1: Power Consumption of Sense Amplifier

Sense Amplifiers	Power Consumption
VMDSA	90.95µW
CMDSA	60.23µW
VLSA	500.78µW
CLSA	200.58µW

VMDSA experiences the least amount of power loss of any SA, as seen in Table 1. Table 2 also demonstrates that when low-power techniques like sleep transistors are used, CMDSA consumes the least power.

Table 2: Power Reduction Techniques over Sense Amplifiers

Techniques Used	Power Consumption			
	VMDSA	CMDSA	VLSA	CLSA
Footer Stack	60.24µW	0.62µW	320.88µW	99.58µW
Sleep Transistor	60.54µW	0.61µW	310.54µW	70.92µW
Sleepy -Keeper	60.85µW	0.60µW	340.21µW	98.57µW

5.0 Conclusion

It was discovered that latch sense amplifiers and current-mode and voltage differential sense amplifiers were used in the study. There were also used other kinds of sensors. The sleep transistor, sleep stack, sleepy keeper, and sleep stack use sensing amplifiers to minimize power usage. The least electricity is used with sleep transistor technology using current mode differential sensing.

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