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Low Power Reduction Techniques Implementation and Analysis in Sense Amplifier Circuit Configurations

*Nitendra kumar Tiwari**

ABSTRACT

MTCMOS (Multi-Threshold CMOS), sleepy stack, sleepy keeper, and footer stack are examples of low power saving techniques incorporated into the core gpdk 90nm technology papers used in the proposed study using Cadence. The main focus of these tests is the power consumption of various sense amplifier circuits. The simulation results show that the charge-transfer sense amplifier uses much less energy than voltage and current sense amplifiers. The present mode detecting amplifier's power consumption can be decreased by up to 98 percent by using MTCMOS technology.

Keywords: *CMSA (current-mode sense amplifier); SRAM (Static random access memory); VMSA (voltage-mode sense amplifier),;Precharge (PCH) circuit; CTSA (charge-transfer sense amplifier).*

1.0 Introduction

Static random-access memory, or SRAM, is essential to modern electronic systems [1]. A typical SRAM device needs all four or six transistors on its grid for exact data processing. The growing need for low-power, noiseless memory has made it evident that SRAM design is essential [2]. The speed at which SRAM can do its jobs is increased by introducing sensing amplifiers. The frequency with which CPUs access their cache and the power consumption of intellectual property in low-power semiconductor devices are significantly impacted by this value [3]. It has been demonstrated that some amplifiers can differentiate between various voltage, current, and charge modes. The time required to generate a new voltage on high capacitance SRAM bit lines is the cause of the VMSA's [4] reduced efficiency. Compared to voltage mode sensing, current mode sensing minimizes the bit line swing of the amplifier during reading. This substantially improves speed and robustness against fluctuations in bit line capacitance. The proposed study would use the Cadence tool to add low-power solutions like the footer stack, MTCMOS (Multi-Threshold CMOS), sleepy stack, and sleepy keeper to the gpdk 90nm technology whitepaper [5].

2.0 The Technique of Reduction of Leakage Power

In this part, we examine the effectiveness of three types of sense amplifiers—charge transfer, current mode, and voltage mode—each with a distinct power profile.

2.1 Footer-stack technique

There is also the MTCMOS method, which is distinct in a few significant ways. The MTCMOS design uses a single PMOS transistor to connect the pull-down n/w to the ground and a

**PhD Scholar, Department of Electronics & Instrumentation, NIT Silchar (E-mail: nitintiwari22@gmail.com)*

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single NMOS transistor to the positive supply voltage (VDD). Because there are two transistors—one on each side—the HVT is massive. Power loss is reduced via distributed discrete transistors compared to a single continuous transistor at the cable's end. The best method for avoiding a blackout is to do this [6].

2.2 Sleepy-stack technique

By combining the stack and sleep operations, the sleepy stack is produced. Here, the two sides of a single transistor are shown. Any of the division transistors can be coupled with a single sleep transistor. When a device is shut off, a sleep transistor breaks the device's connection to the earth and the network's power supply [7]. The device then runs out of power. The thick-stack approach uses the stacked transistor to lower the output current. Even when the sleep transistors are disabled, the logic state of the sleepy stack is unaffected. For at least two different causes, the formation of the sleepy stack might have decreased the outflow. The local electricity consumption has been significantly decreased through parallel and high-power transistors. An external source supplies electricity to the sleep transistor.

2.3 Sleepy-keeper technique

A series connection between a PMOS pull-down sleep transistor and an NMOS pull-up sleep transistor is used to achieve this result. By connecting two transistors in parallel to VDD and ground, the n/w is dragged up and down (GND). This method can build a low-power, compact architecture without compromising the circuit's dependability [8]. The pull-up n/w and the NMOS transistor attached to VDD are turned on when the device is in sleep mode. As a result, the information value will continue to be 1. Pull-down n/w and GND keep the PMOS transistor's ON state active. This enables safe standby data archiving.

2.4 MTCMOS

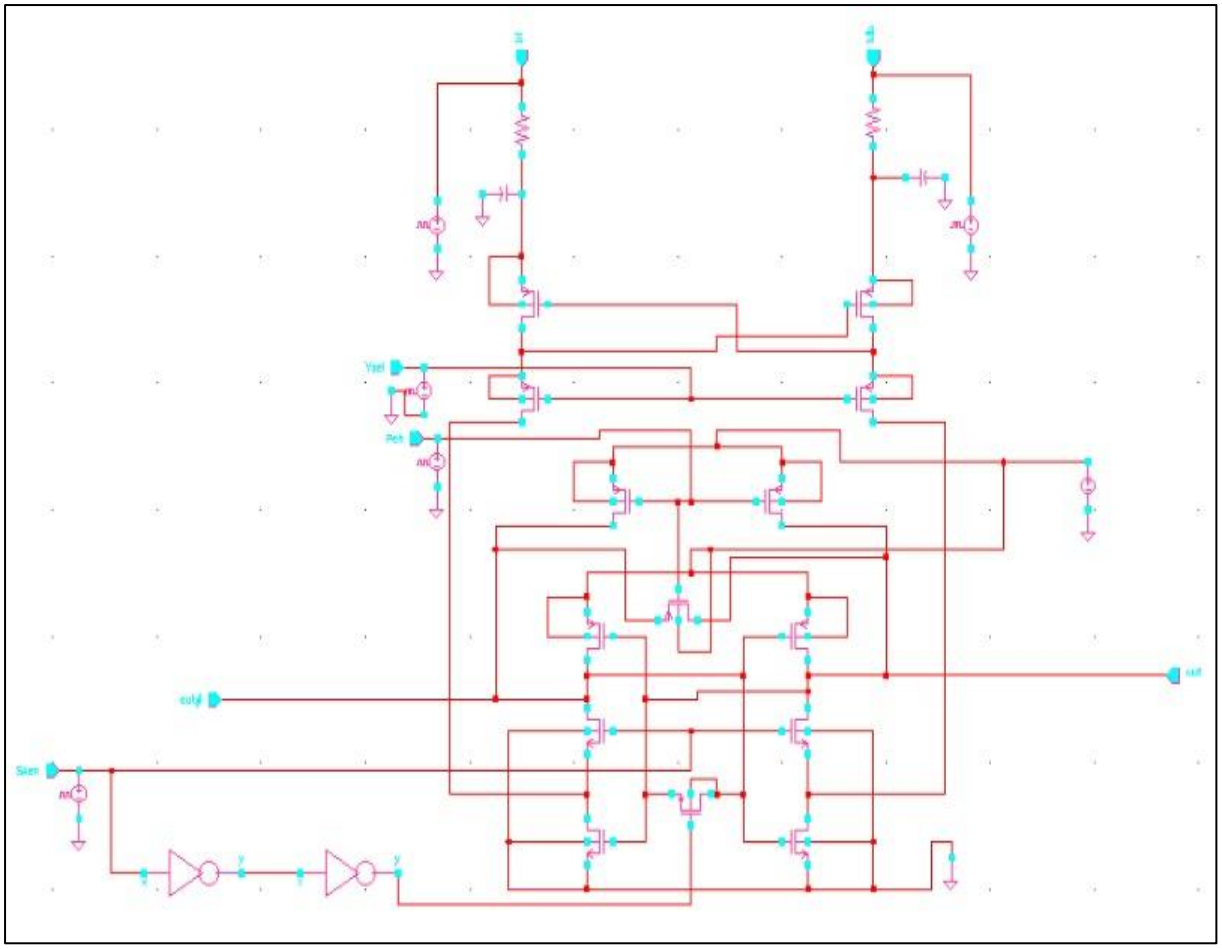
The [6] approach can be applied in static or dynamic environments. Throughput can be raised by decreasing threshold voltages in the stochastic implementation, while leakage power can be minimized by raising voltages at components along the crucial route. The dynamic realization lowers the threshold voltages of the operational blocks connected to the virtual GND line [9]. This line could be connected to the system's ground supply due to the high threshold voltage of the sleep transistor. The operational block might be able to finish its tasks more quickly because of its low Vth and sleep signal being switched on while it is operating. Cutting the length of the design cycle helps lower leakage current. The sleep signal disables the high Vth transistor when the device is in standby mode. As a result, it is now possible to use the virtual GND line. This strategy has several different names.

3.0 Sense Amplifier Circuits

3.1 Current-mode sense amplifier

The CMSA keeps track of how much power each of the device's bit cells uses. The voltage between the bit lines is not required for any purpose. This permits a lower clamp voltage on the low-going bit line than a VMSA. As a result, the bit line can be charged more quickly and effectively. The architecture of the CMSA comprises a differential current-detecting sensor circuit and a current-carrying channel having unity gain current transfer characteristic. Figure 1 shows a reduced version of the internal design of the CMSA. In this case, concepts from [10] have been blended.

Figure 1: CMSA Diagram



3.2 Voltage- mode sense amplifier

Figure 2 shows the standard VMSA circuit, and the process did not proceed as expected. The VMSA has developed a novel technique for determining the voltage difference that entails depleting the bit lines' capacitance. The bl/blb pair experiences a voltage difference when W L is turned on. The technology and circuit activate the sensing amplifier when the gap is significant enough to allow (SAen). The differential output of the inverters can then be converted to full rail output via a positive feedback loop [11]. The low-voltage bit line (V1), which is grounded, is connected to one of the sensing amplifier's outputs nodes.

The voltage at V2, the other output node, is kept constant. The sensing amplifier is turned on when the saturation point is achieved by N MOS devices N1 and N2. The N MOS device N2 draws greater current when operating at full VDD despite having a lower Vgs voltage than the N1 device. The output voltage of the first NMOS device increases due to its higher current conductivity (N1), whereas the output voltage of the second N MOS device drops. Before the N MOS device N2 enters the linear zone and the P MOS device P1 is turned on and driven high, the voltage at the input of the other inverter, V1, must drop below a threshold level. The cross-coupled inverters store the output for subsequent use when N1 is turned off.

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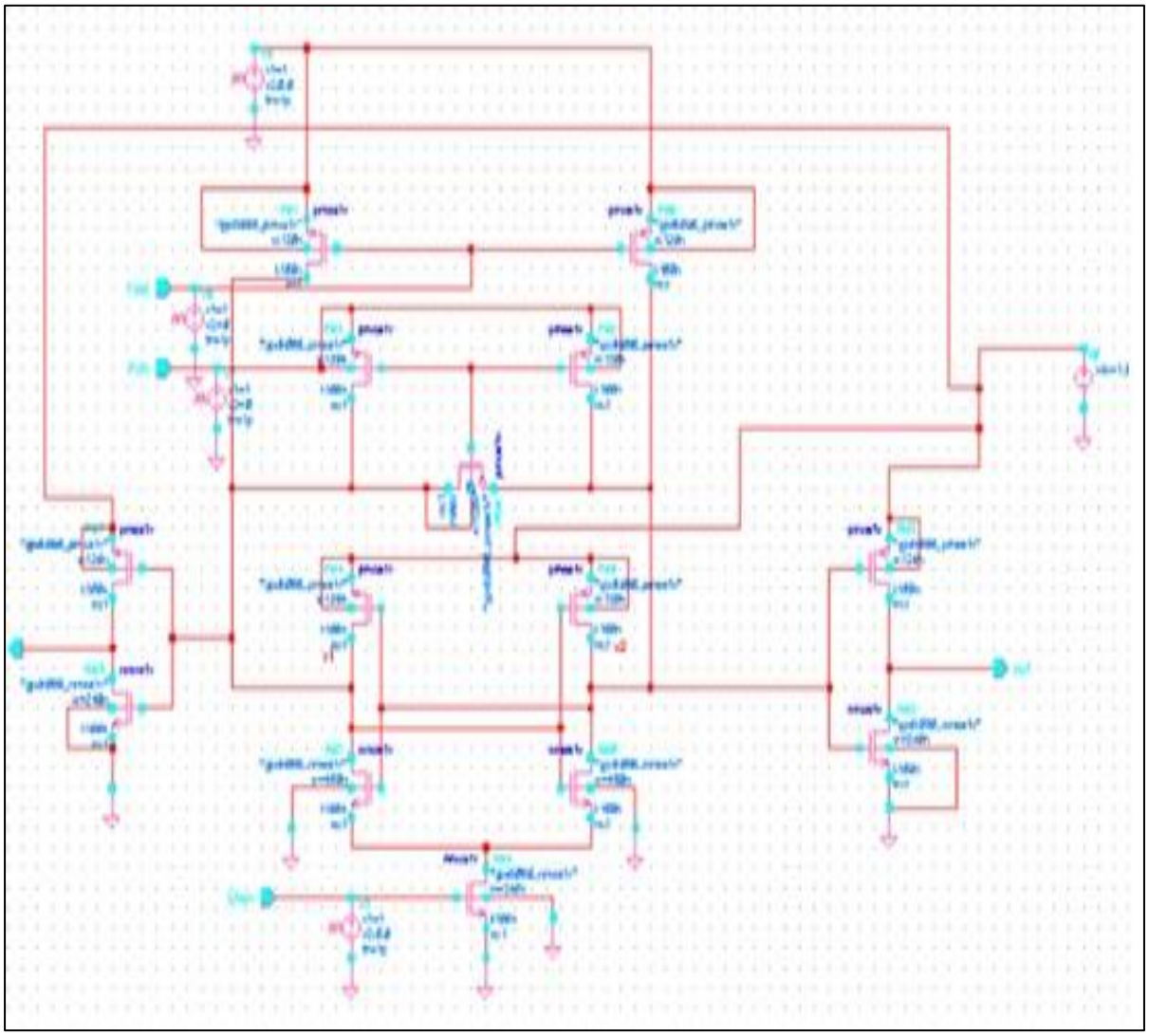
Figure 2: VMSA Diagram



3.3 Charge-transfer sense amplifier

The CTSA enables quick data transmission by moving charge from high-capacitance bit lines to low-capacitance Sense Amplifier outputs. The voltage swing on the bit lines is inversely correlated with the power and speed of a computer [12,13]. Refer to Figure 3 to learn more about how CTSA functions.

4.0 Results and Discussion

Compared to the voltage mode sense amplifier and the current mode sense amplifier, the charge transfer sense amplifier only uses 11.069μW of power (Table 1). Current mode sensing amplifiers can take advantage of the footer-stack, metal-oxide-semiconductor (MOS), sleepy-stack, and sleepy-keeper low power reduction approach since they significantly reduce power loss. Reductions of 99%, 94%, and 98%, respectively (Table 2).

Figure 3: CTSA Diagram

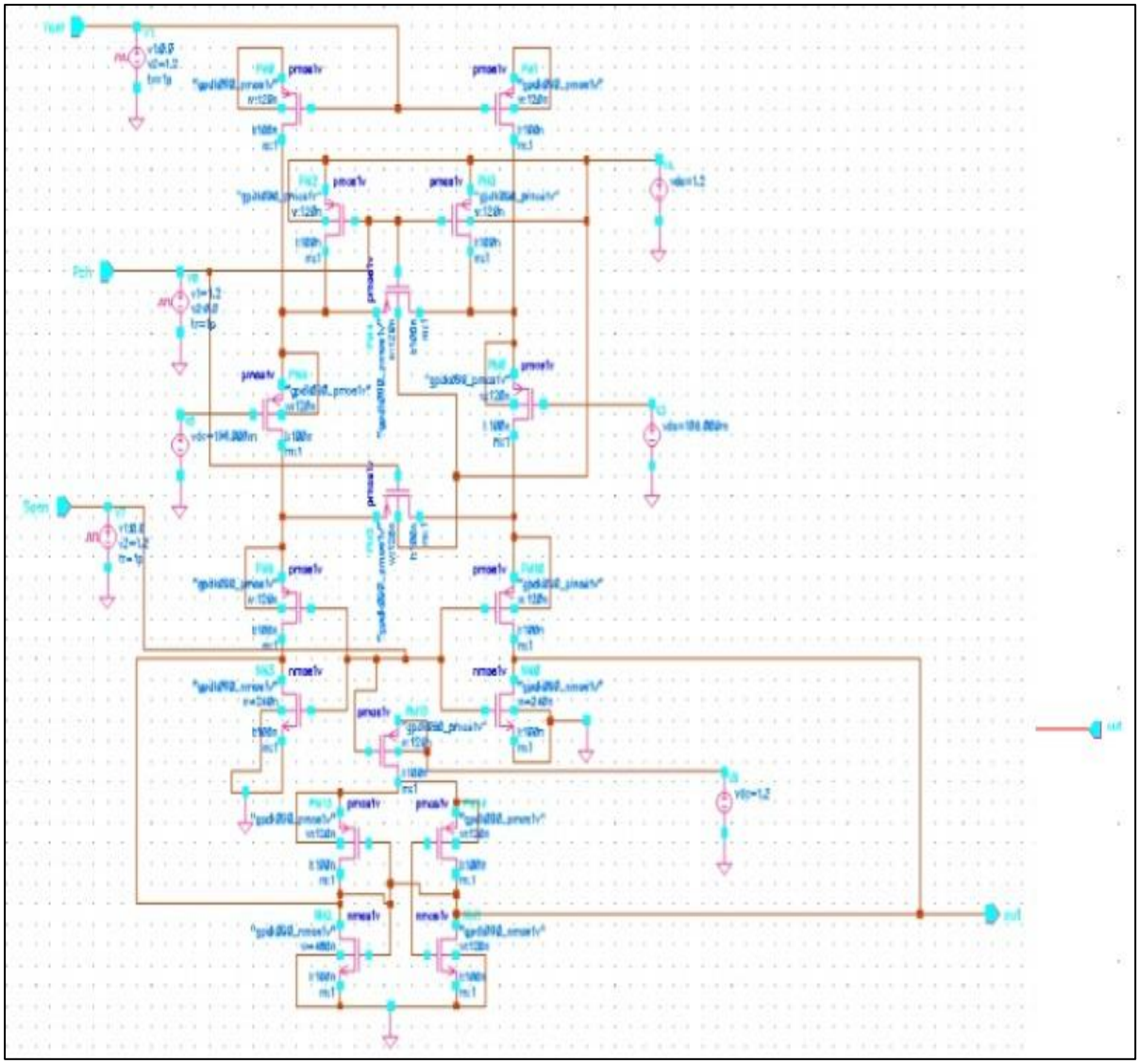


Table 1: Power Consumption of Sense Amplifiers

Sense Amplifiers	Power Consumption
Current-Mode Sense Amplifier	60.30µW
Charge-Transfer Sense Amplifier	20.21µW
Voltage-Mode Sense Amplifier	90.87µW

Table 2: Different Sense Amplifier Leakage Techniques Affect Power Consumption

Techniques Used	CMSA	VMSA	CTSA
Sleep-Stack Technique	3.52µW	70.28µW	3.88µW
Footer Stack Technique	0.62µW	60.55µW	3.38µW
Sleepy-Keeper Technique	0.66µW	60.20µW	3.55µW
MTCMOS Technique	0.61µW	60.21µW	3.43µW

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5.0 Conclusions

Numerous amplifiers for sensing voltage, current, and charge transfer were built to conduct the suggested research using 90ηm CMOS technology and low power reduction techniques. According to research, the footer stack strategy is the best way to reduce power usage, outperforming MTCMOS, Sleepy-Stack, and Sleepy-Keeper in every area. As a result, power loss in the current sense amplifiers is reduced. Voltage and current sense amplifiers are inferior to charge transfer sense amplifiers. The peak speeds and thrust levels of the CTSA and VMSA are comparable. For CMSA to move faster than CTSA, more energy is required.

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