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A 0.18µm Low Power, High Speed Ternary Content Addressable Memory

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ABSTRACT

Ternary content addressable memory or associative memory have their primary application in Network Router. In today's all web based search engine TCAM memory is employed. But power consumption is a major issue with a TCAM. In this paper a lowpower ternary content addressable having very low leakage is proposed. Simulation results shows upto 30% reduction in power. The circuit has been deesigned and implemented in 0.18 µm CMOS technology. The circuit dissipated a maximum 10.5 nW of power and is suitable for low power application.

Keywords: *Power Dissipation; Leakage; Speed; TCAM.*

1.0 Introduction

An efficient hardware solution to perform table lookup is the ternary content addressable memory (TCAM). TCAM searches for matching data by content and returns the address at which the matching data is found. TCAMs are used extensively today in applications such as network address translation, pattern recognition, and data compression. In these applications, there is a steady demand for TCAMs with higher density and higher search speed, but at constant power. Currently, commercial TCAMs are limited to 18 Mb of storage and 100 million searches per second on a 144-bit search word, at typically 5 W per TCAM chip. Compared to the conventional memories of similar size, TCAMs consume considerably larger power. This is partly due to the fully parallel nature of the search operation, in which a search word is compared in parallel against every stored word in the entire TCAM array.

A TCAM can be used as a co-processor for the network processing unit (NPU) to offload the table lookup tasks. Besides the networking equipment, TCAMs are also attractive for other key applications such as translation look-aside buffers (TLBs) in virtual memory systems [1-2], tag directories in associative cache memories [3-4], database accelerators [5], data compression [6], and image processing [7]. Recent applications of TCAMs include real-time pattern matching in virus/intrusion-detection systems and gene pattern. searching in bioinformatics [8-9]. Since the capacities and word-sizes of TCAMs used in most of these applications are much smaller than the TCAMs used in networking equipment, the current TCAM research is primarily driven by the networking applications, which require high capacity TCAMs with low-power and high-speed operation.

2.0 Proposed Low Power High Speed Cell

The proposed low power circuit has shown in Fig. 1. This TCAM cell use two independent cell for storing '1' , '0' and 'X'. 'X' is mask state. The crcuit uses AND type match line. Transistor 11 and 12 store complementary valuewhen store word is either 0 or 1. Transistor 5 and 7 are used to charge node between search

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line. Transistor 11 and 12 perform the comparaision operation i.e. XOR operation.

The static power of CMOS circuit is given y equation (1)

$P_S = I_L * V_{DD}$ … (1)

Where,

IL= Leakage current of the circuit

The subthreshold leakage current of NMOS transistor with zero V_{GS} voltage and full swing V_{DS} is given by equation (2) [9]

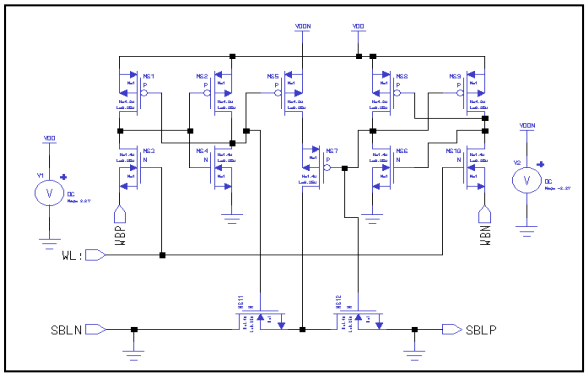
$$I_{SV} = I_o \exp\left(-\frac{K_1\sqrt{\phi_s} - K_2\phi_s - \eta V_{dd}}{nV_r}\right) \quad (2)$$

Where,

$$I_o = \mu_o C_{ox}\left(\frac{W_{eff}}{L_{eff}}\right)Vr^2 e^{1.8}$$

η = barrier lowering parameter
K_1, K_2 = no uniform doping effect parameer
V_T = thermal voltage = KT/q
μ_0 = mobility of elctron
L_{eff} = channel length of transistor
W_{eff} = channel width of transistor
Equation (2) shows an exponential relation between I_{SN} and V_{DD}.

Fig 1: Proposed Circuit



The Current Density Dye to Direct Tunneling is Given By (3)

$$J_{DT} = AE_{ox}^2\left(\frac{\phi_{ox}}{V_{ox}}\right)\left(\frac{2\phi_{ox}}{V_{ox}} - 1\right)e^{\frac{B[1-(1-\frac{Vox}{\phi ox})^{3/2}]}{Eox}} \quad (3)$$

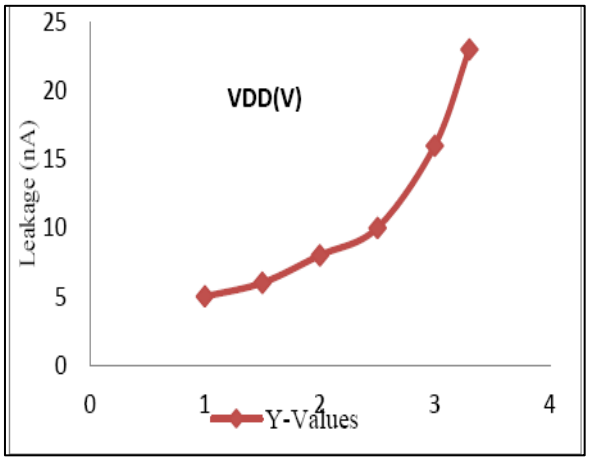
Where, $A = \frac{q^3}{16\pi^2 h\phi_{ox}}$ and $B = \frac{4\sqrt{2m^*}\phi_{ox}^{3/2}}{3hq}$

V_{ox}= voltage drop across the oxide
Eox = ekectric field in the oxide
Tox = oxide thicknss
M* = effective mass of an electron
H= plank costant

3.0 Results and Discussion

The proposed Low Power Ternary Content Addressable Memory circuit has been designed and implemented in 0.35µm CMOS technology. The minimum supply voltage is 1.5 V and the maximum supply current is 11.5µA at the maximum supply voltage of 2.5 V and the maximum temperature of operation is 300^0K. The circuit simulation results are presented in Fig. 2.

Fig 2: TCAM Cell Leakage for 0.18 µm Technology



4.0 Conclusions

A TCAM circuit has been proposed and simulated results has been discussed. The simulation results show that the circuit is highly immune to supply and temperature variation. Simulation result shows upto 30% reduction in leakage and cell area over the conventional TCAM cell. This circuit can be used in network routers, search engine and other low-power applications.

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