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Adaption of Power Gating in Positive Feedback Adiabatic Logic Circuits

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ABSTRACT

Positive Feedback Adiabatic Logic (PFAL), a quasi static and differential logic adiabatic family, is one of the most robust, with significant reduction in power consumption has been chosen in this work. Power Gating has been adapted in order to further reduce power dissipation. It is accomplished by sleep state control units that switch circuits between awake and idle. Two power gating methodologies, footer and header, have been evaluated and compared. The functional verification and power evaluations have been performed using TSPICE simulations with 180nm TSMC CMOS parameters. Power consumption has also been examined by varying supply voltage, frequency of the power clock signal and load capacitance. The observed overhead in awake state power dissipations is compensated for with the significant decrease in idle state power dissipation.

Keywords: *Adiabatic Logic; Low power; VLSI; Power Gating.*

1.0 Introduction

Excessive and continual use of portable electronics like smartphones, tablets and laptops is the norm of today's world. With electronic devices penetrating every part of our life right from the early morning news on a tablet to late night chat on our smart phones, longer battery lifetime is the need of the hour [1]. Power dissipation of the circuit, being the most important factor dictating its battery lifetime, is desired to be as low as possible. Low power VLSI design is thus, a very crucial step in design of modern electronics [2].

Many techniques like voltage scaling and shrinking feature size have been employed in static CMOS, the most popular logic family in IC design, which help in reducing power dissipation [1]. CMOS logic suffers from primarily three factors of power dissipation, dynamic (switching), static and short circuit power dissipation. The dynamic power dissipation is directly proportional to the input frequency, thus the former increases with an increase in the latter [2]. Recent devices perform extremely fast computations and processes, as they are designed to work at higher frequencies, hence dissipate large amounts of power. Adiabatic logic is yet another logic style wherein charge is recovered back to power supply from the load capacitance. Therefore, thislogic style has great potential to reduce power dissipation beyond the limit imposed by static CMOS logic style [3].

Adiabatic logic design reduces power dissipation drastically. This logic provides a method to utilize the energy stored in load capacitors unlike the traditional way of wasting the energy stored in load capacitor by discharging it to the ground. Different topologies of adiabatic circuit designing has been developed, they use sinusoidal or four phase trapezoidal power supply [4].

With the advent of modular designing and different circuits combining to together function as a whole unit, there is a lot of power wasted on the sub-circuits that are not computing at each instant of time [5].

Therefore these sub-circuits can be turned off while they are not contributing anything to the whole unit,this is achieved by introducing Power Gating in the circuit. Two methodologies for power gating have been employed in this paper, namely, header and footer, specifically on adiabatic full adder circuits because of their wide range of applications [1]. Adders are used in a variety of application ranging

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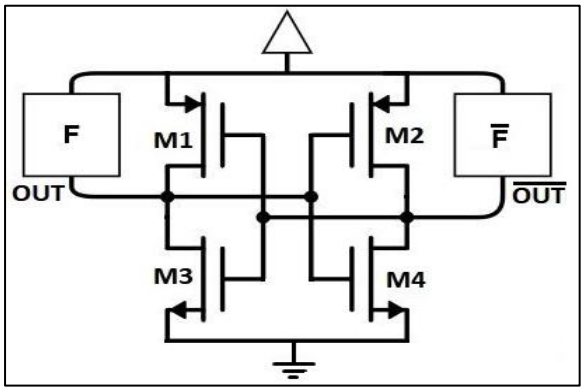
frombasic arithmetic blocks to advanced systems like DSP, filtering and image processing [6].

This paper is organized in seven sections including the introductory one. The second section discusses about Positive Feedback Adiabatic Logic Family which has been studied in detail for power evaluations. Section 3 sheds light on methods to further minimize power in adiabatic circuits. This section discusses about the two gating methods used to design circuits. The fourth section briefly discusses about full adders. Section 5 comprises of the functional verifications andpower evaluations. Conclusions have been drawn in the next section followed by references in the last section.

2.0 Positive Feedback Adiabatic Logic (PFAL)

The PFAL family consists of a latch made by two cross coupled inverters (M1, M2, M3 and M4), which provides the positive feedback [7]. The generic cell of PFAL is show in Fig.

Fig 1: Generic Cell of Pfal

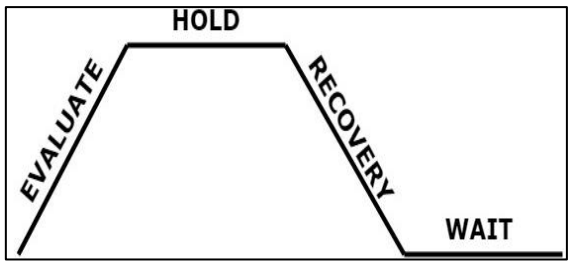


It generates both the output and its complement when both input and complement of input is applied. The NMOSs M3, M4 and PMOSs M1, M2 form the cross coupled inverters that drive the two complementary outputs. The two NMOS networks F and its complement F act as the pull up networks in the PFAL family. When the function block F is active the output OUT is charged and its complement OUT is discharged and vice versa for when function block $\overline{F}$ is active.

PFAL is one of the adiabatic logic families that use a four phase trapezoidal power clock as shown in Fig.2. The adiabatic families make use of sinusoidal or trapezoidal power supply [8].

The four phases are evaluate phase, where the actual computation of output takes place, hold phase for holding the output stable for the next cascaded block, third phase is the when the charge is recovered from load capacitance back tosource hence it is called recovery phase, finally the last wait phase has been introduced to maintain symmetry, in this phase both output nodes remain discharged [1,8].

Fig 2: Four Phase Trapezoidal Clock



3.0 Further Power Reduction

Techniques like voltage scaling, transistor sizing, power gating and shrinking feature size have been employed to reduce power dissipation [9]. Power gating being a coherent and robust has been adapted to PFAL, here state control transistors are used to switch circuit between active and ideal states. Two different gating methods, header and footer, have been mentioned in this work employed using a full adder [10]. Power gating is an approach to occasionally turn off the circuits, by isolating one of the power rails Vclk or ground which are not operational [1,10]. The generic cell of a power gated PFAL family is shown in Fig.2.

Fig 3: Generic Cell of a Power Gated PFAL Family

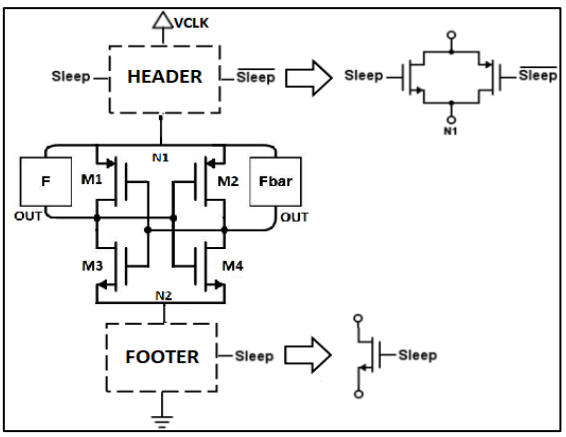


Figure 2, shows footer sleep state control unit which has a NMOS connected to the main circuit and the ground, as it required for passing a strong low (0V) [3]. This NMOS creates a virtual ground on Node N2 in awake state whereas in the idle state, this node N2 becomes a floating state [3, 11]. Similarly, the header sleep state control unit is a transmission gate (TG) for passing the trapezoidal clock, which consists of both high and low voltage signals, so as to create a Virtual Vclk at node N1 in awake state and no charging path in idle state [3, 11].

4.0 Low Power Full Adder

Full adders are rudimentary yet extremely salient building blocks of any digital system. Thus we initiate the efforts for more efficient full adders in terms of performance, accuracy, power requirements, speed and flexibility. The modern day devices are moving towards digitization and fast data computation [12]. An adder is a potent circuit that performs addition of numbers. Addition is a basic operation used to realize complex mathematical operators like integration, differentiation and equations utilizing subtraction, multiplication and division which can be implemented by monitored use of adders in a particular way, hence an adder plays a vital role in all computations [12]. With the demand for high speed processing and low power design being accelerated by expanding computer and signal processing applications, it makes adders even more important. Adders are used as basic building blocks in DSP systems, filtering, digital image processing and machine learning applications [12]. A full adder is a three input-two output adder, where the two outputs are denoted as Sum and C_{out} (CARRY), with inputs A, B and the input carry C [13]. The governing equations for functionality of a full adder are given in (1) and (2)

$$SUM = A \oplus B \oplus C \quad \ldots (1)$$

$$CARRY = A.B + B.C + C.A \quad \ldots (2)$$

Sum is implemented as exclusive-OR of the three inputs of the full adder and the output Cout is implemented as mentioned in Eqn. 2. PFAL based Full adder implementation is depicted in Fig.4.

5.0 Simulation Results

This section entails the functional verification of PFAL based Full Adder of Fig. 4 and its gated version obtained by applying the concept given in Fig. 3. The technology node of 180 nm TSMC CMOS is considered and a trapezoidal power clock of frequency 200MHz is applied.

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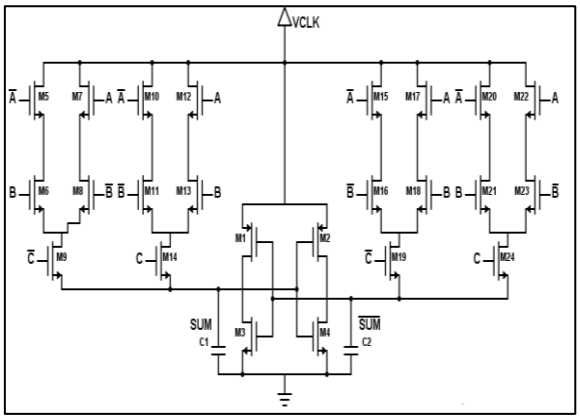
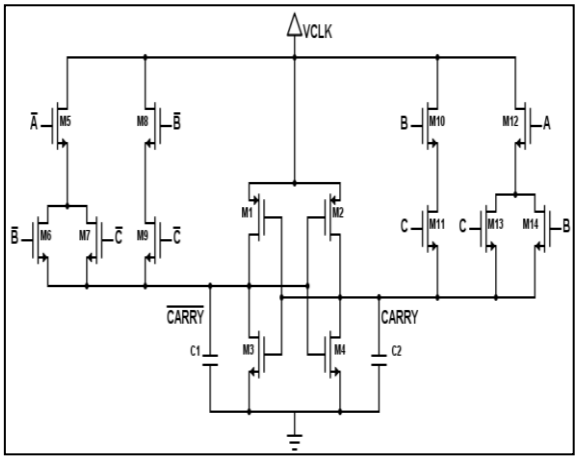
Fig 4: Schematic of PFAL based Full adder (a) Sum (b) Cout5. Simulation Results

(a)



(b)

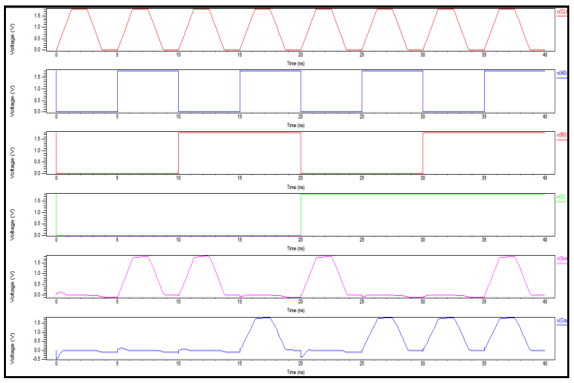


5.1 Functional Verification

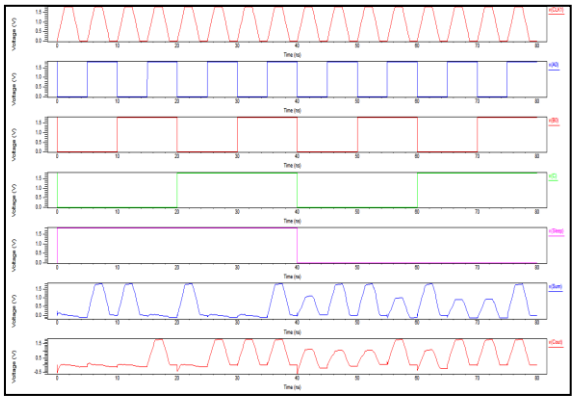
The time domain simulation of PFAL based un-gated Full adder, footer gated and header gated full adder functions are placed in Fig. 5. In awake state i.e. Sleep signal is high and the output follows the full adder functionality whereas for a low on sleep makes output in floating state/ grounded for footer/ header gated scheme.

Fig 5: Time Domain simulation Waveforms for (a)un-gated, (b)Footer gated and (c) Header Gated PFAL Based Full adder

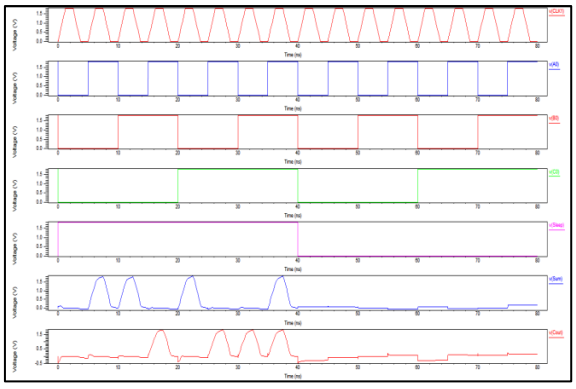
(a)



(b)



(c)



5.2 Variation of power dissipation with load capacitance

The evaluations have been performed at a power supply of 1.8V and a constant input frequency of 200 MHz for full adder. The results have been in compiled in graph in Fig.6

The power dissipation of the gated PFAL full adder is measured for various load capacitances ranging from 10fF to 80fF. Power dissipated increases with increase in load capacitance. Gated circuit in active state consume more power than its ungated counterpart throughout the range of capacitances.

5.3 Variation of Power Dissipation with Supply Voltage

The evaluations have been performed at a load capacitance of 10fF and a constant input frequency of 200 MHz for full adder. The results have been in compiled in graph in Fig.7

Fig 6: PFAL based Full Adder Power Dissipation w.r.t Load Capacitance

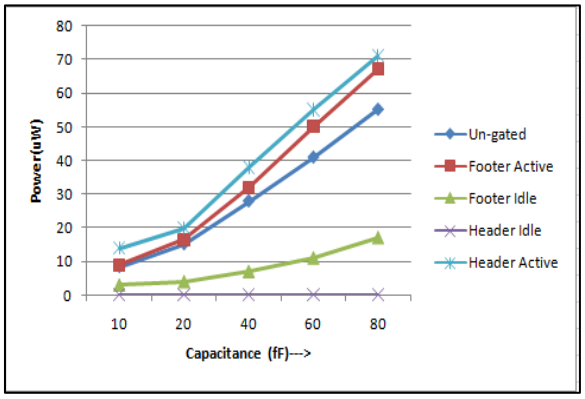
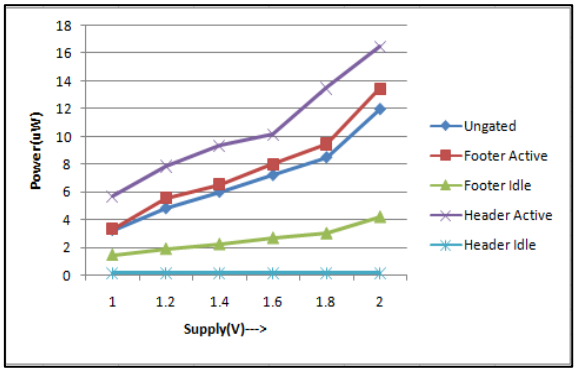


Fig 7: PFAL Based Full Adder Power Dissipation w.r.t Supply Voltage

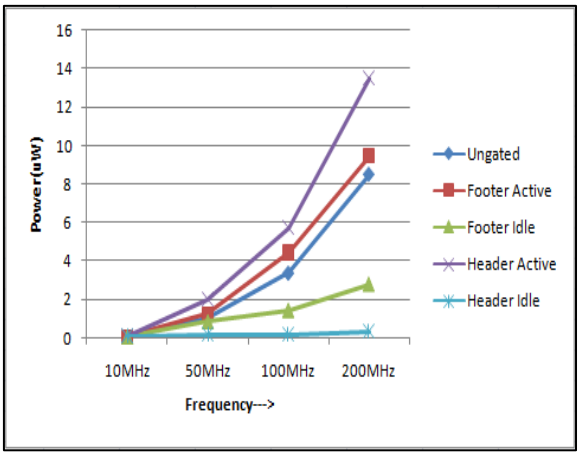


The graph shows the increasing trend of the power dissipation with supply voltage, with gated active circuits dissipating more power than ungated counterpart, with header active circuits consuming notably more power. On the other hand, header idle circuits dissipate negligible power as compared to footer idle.

5.4 Variation of Power Dissipation with Input Frequency

The evaluations have been performed at a power supply of 1.8V and a constant input frequency of 200 MHz for full adder. The results have been in compiled in graph in Fig.8

Fig 8: PFAL based Full Adder Power Dissipation w.r.t Input Frequency



As seen in the graph the power dissipation increases with frequency and a sharp rise is observed after 100MHz. Similar trend is observed here with with header idle circuits having negligible dissipation while its active state has largest power dissipation. The footer gated circuits have less active power than header but there is significant dissipation in idle state.

6.0 Conclusions

In the present paper, full adder has been implemented using ungated and gated topologies of PFAL. The performance of the full adder has been evaluated using 180nm TSMC parameters on TSPICE.

The variation of power consumption with load capacitance, input frequency and supply voltages In the present paper, full adder has been implemented using ungated and gated topologies of PFAL. The performance of the full adder has been evaluated using 180nm TSMC parameters on TSPICE. The variation of power consumption with load capacitance, input frequency and supply voltages depict that the gating in adiabatic circuits further reduces power up to a large extent.

The observed overhead in awake state power dissipations is compensated for with the significant decrease in idle state power dissipation, with footer gated structures having approximately one fourth power dissipation in idle state as compared to its ungated counterpart. Whereas header gated structures have almost negligible idle state power consumption. Power saving has been achieved remarkably in the proposed power efficient 1-bit full adder using gated PFAL.

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