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Single-Input Dual-Output Three-Level DC–DC Converter for EV

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ABSTRACT

This paper presents the development of a non-isolated single-input dual-output three-level dc–dc converter (SIDO-TLC) appropriate for medium- and high-voltage applications. 3 level Buck-Boost converter is used in order to achieve the controllable output voltages. The main merits of this project include reducing voltage stress across semiconductor devices, improving efficiency, and reducing passive components size. This converter shows very good stability, even under simultaneous step changes of the loads and input voltage. Simulation analysis of converter output voltages for various duty cycles is presented for three cases of duty cycle control range.

Keywords: *Multiple converter; Single input dual-output dc-dc converter (SIDOC); Single-input dual-output three-level dc-dc converter (SIDO-TLC); Buck-boost converter.*

1.0 Introduction

Multi-Output DC-DC converters have attracted increasing interest due to the high demand for energy in many fields and for different applications, such as supplying different loads at the same time and the integration of renewable energy sources (photovoltaic panels, wind turbine, etc.) in micro-grids. At higher voltages, switches voltage stress is a major challenge for multiport dc–dc converters. The reason for that are the issues such as the cost and the inaccessibility of high-voltage switches, which could also have a negative effect on overall efficiency. The project is about designing a high-efficiency multiport dc–dc converter with reduced voltage stress across semiconductor devices and shrunken passive components size. K. Filsoof and P. W. Lehn [2] proposed a bidirectional multiple-input multiple-output modular multilevel DC–DC converter and its control design. In this converter, the voltage stress on switches is shared among the levels. In addition to its complex control system, the converter is not capable of generating buck and boost output voltages at the same time. As a result, it requires two separate circuits with different topologies to generate each voltage separately. O. Ray, A. P. Josyula, S. Mishra, and A. Joshi [3] proposed integrated dual-output converter. Proposed converter which one of its outputs is boost and the other one is buck at the same time. The converter is appropriate for low-voltage applications. Meanwhile, because of high voltage stress on the diode and the series added switches, and also due to the lack of proper high input current distribution among the switches, the converter's both conduction and switching losses are high, which can lead to a fairly low system efficiency. SEPIC based

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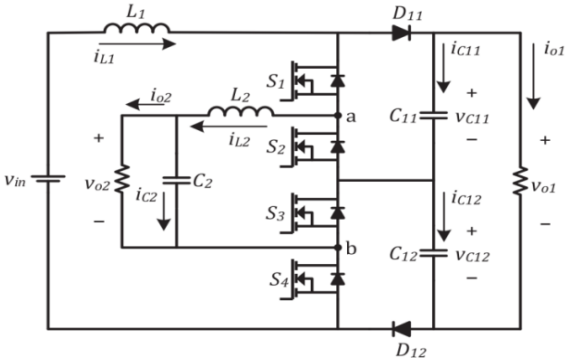
dual output DC-DC converter for solar applications is proposed in [4]. The converter which is a combination of the SEPIC and five-level boost converters is composed of one switch and ten diodes. The voltage stress on the switch is reduced to one-fifth of the high voltage side. Yet, high number of diodes may effect the reliability of the system. Moreover, reducing the passive components size, which is one of the advantages of the multilevel structures, has not been achieved through the proposed converter.

This paper presents the modeling and performance of single-input dual-output DC-DC converter. Simulation results are presented to demonstrate the buck and boost utput voltage ranges under three cases of duty cycle control range.

2.0 Single-input Dual- Output Three- Level Dc- Dc Converter

Figure 1 shows the circuit diagram of the Single-Input Dual-Output Three- Level DC-DC Converter. In Figure 1, Vin is the input voltage, Vo1 is the step-up output voltage, Vo2 is the step- down output voltage. The series capacitors C11 and C12 are the filter capacitors of the step-up output, while C2 is that the filter capacitor of the step-down output. The converter consists of 4 power switches: S1, S2, S3, and S4, with antiparallel diodes, and two power diodes: D11 and D12. Vab is that the unfiltered step-down output voltage, VL1 and VL2 are the instantaneous voltages of inductors, iC11 and iC12 are the currents of the series capacitors, iC2 is the current through the step-down capacitor C2, and VC11, VC22 are the voltages of the series capacitors and VC2 is the voltage of the step-down capacitor.

Figure 1: Circuit Diagram of SIDO-TLC



2.1 Switching states of single- input dual-output three-level DC-DC converter

Table 1 shows the switching states, the unfiltered step-down output voltage Vab, the instantaneous voltages of inductors VL1 and VL2, the currents of series capacitors iC11 and iC12, and also the voltage change (direction) of capacitors.

2.2 Operating range of single-input dual-output three-level DC-DC converter

Regarding the duty cycles of the switches, there are three possible operating cases named A, B, and C

Table 1: Operating Range of the Sido-TLC

Switching States	S_1	S_2	S_3	S_4	V_{ab}	V_{L1}	V_{L2}	i_{c11}	i_{c12}	C_{11}	C_{12}
1	0	0	0	0	0	V_{in}-V_{o1}	-V_{o2}	i_{L1}-V_{o1}/R_{o1}	i_{L1}-v_{o1}/R_{o1}	↑	↑
2	0	0	1	0							
3	0	1	0	0							
4	0	1	1	0							
5	0	0	1	1	0	V_{in}-V_{o1}/2	-V_{o2}	i_{L1}-v_{o1}/R_{o1}	-V_{o1}/R_{o1}	↑	↓
6	0	1	1	1							
7	1	1	0	0	0	V_{in}-V_{o1}/2	-V_{o2}	-V_{o1}/R_{o1}	i_{L1}-v_{o1}/R_{o1}	↓	↑
8	1	1	1	0							
9	0	0	0	1	V_{o1}/2	V_{in}-V_{o1}	V_{o1}/2-V_{o2}	i_{L1}-v_{o1}/R_{o1}	i_{L1}-i_{L2}-V_{o1}/R_{o1}	↑↑	↑
10	0	1	0	1							
11	1	0	0	0	V_{o1}/2	V_{in}-V_{o1}	V_{o1}/2-V_{o2}	i_{L1}-i_{L2}-V_{o1}/R_{o1}	i_{L1}-v_{o1}/R_{o1}	↑	↑↑
12	1	0	1	0							
13	1	0	1	1	V_{o1}/2	V_{in}-V_{o1}/2	V_{o1}/2-V_{o2}	i_{L1}-i_{L2}-V_{o1}/R_{o1}	-V_{o1}/R_{o1}	↑	↓
14	1	1	0	1	V_{o1}/2	V_{in}-V_{o1}/2	V_{o1}/2-V_{o2}	-V_{o1}/R_{o1}	i_{L1}-i_{L2}-V_{o1}/R_{o1}	↓	↑
15	1	0	0	1	V_{o1}	V_{in}-V_{o1}	V_{o1}-V_{o2}	i_{L1}-i_{L2}-V_{o1}/R_{o1}	i_{L1}-i_{L2}-V_{o1}/R_{o1}	↑	↑
16	1	1	1	1	0	V_{in}	-V_{o2}	-V_{o1}/R_{o1}	-V_{o1}/R_{o1}	↓	↓

for the SIDO-TLC. In the ideal situation, the control signals of S1 and S4 have the same duty cycles (dS1 = dS4 = d1) and are 180° phase shifted. In the same way, the control signals of S2 and S3 have the same duty cycles (dS2 = dS3 = d2) and are 180° phase shifted. Depending on d1 and d2 values, the operating cases can be expressed as follows:

Case A: (1/2 < d1 and d2 < 1) and (d1 > d2)
Case B: (1/2 < d1 and d2 < 1) and (d1 < d2)
Case C: (d2 + 1/2 < d1 < 1) and (0 < d2 < 1/2).

Table 2: Operating Range of The Sido-TLC

CASE	Duty-cycle limits	Voltage limits
A	½ < d_1 & d_2 < 1 $d_1 > d_2$	$v_{in/2} < v_{o2} < v_{o1/2}$
B	½ < d_1 & d_2 < 1 $d_1 < d_2$	0< v_{o2} < $v_{in/2}$ v_{o1}> 2(v_{in}-v_{o2})
C	d_2 + ½ < d_1< 1 0< d_2 < ½	$v_{o1/2}$<v_{o2}<v_{01} v_{in}< v_{o1}< 2v_{in}

2.3 Waveforms (different cases) of single-input dual – output three-level DC- DC converter

3.0 Mathematical Modeling of SIDO-TLC

According to switching states of SIDO-TDC and the switching sequences in waveforms, the output voltage's conversion ratio can be obtained.

3.1 Case A

For inductor L_1,

$\underline{V_{in}(d_2-1/2)} + \underline{(V_{in}-V_{o1}/2)(d_1-d_2)} + \underline{(V_{in}-V_{o1})(1-d_1)}=0$

State 16 State 13 State 12

$V_{in}(d_2)-V_{in}/2+V_{in}(d_1)-V_{in}(d_2)-$
$V_{o1}(d_1)/2+V_{o1}(d_2)/2+V_{in}-V_{in}(d_1)-V_{o1}+V_{o1}(d_1)=0$
$V_{in}=V_{o1}(2-d_1-d_2)$
$V_{o1}/V_{in}=(1/2-d_1-d_2)$ …(1)

Therefore, Step-up voltage gain = V_{o1}/V_{in}=1/(2-d_1-d_2).

For inductor L_2,

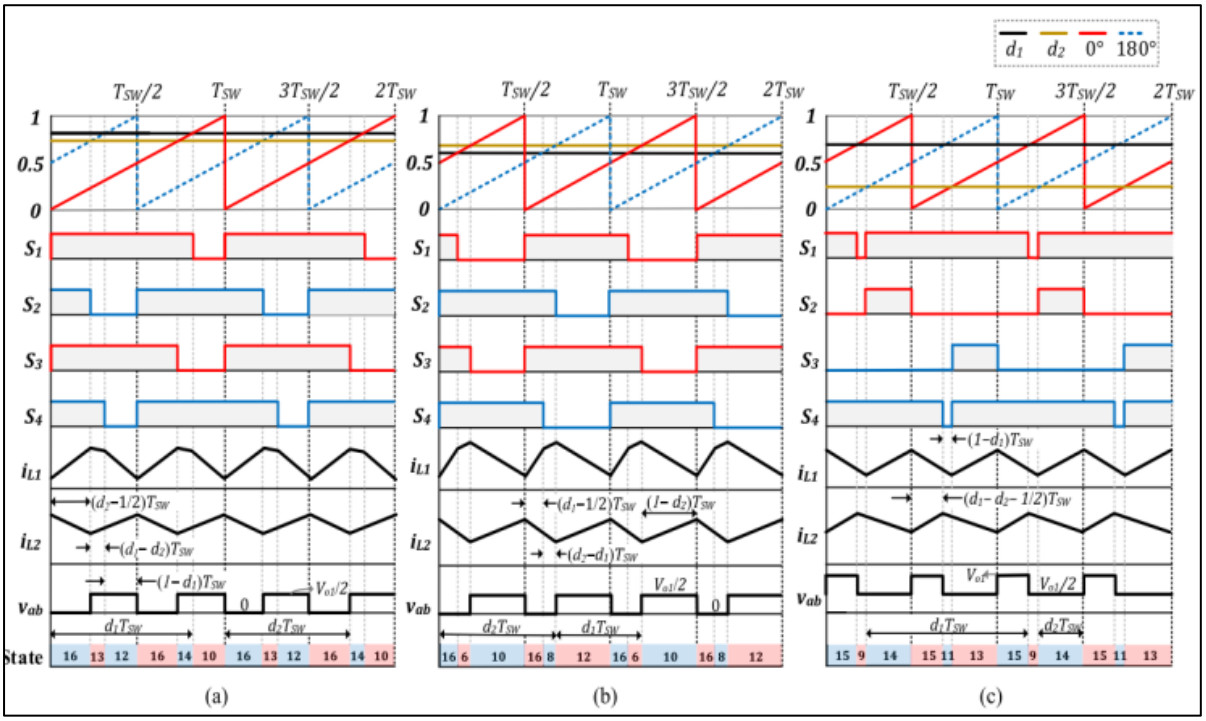
$\underline{(-V_{o2})(d_2-1/2)}+\underline{(V_{o1}/2-V_{o2})(d_1-d_2)}+\underline{(V_{o1}/2-V_{o2})(1-d_1)}=0$

state 16 state 13 state 12

$-V_{o2}(d_2)+V_{o2}/2+V_{o1}(d_1)/2-V_{o1}(d_2)/2-V_{o2}(d_1)+V_{o2}(d_2)-$
$V_{o1}(d_1)/2+(V_{o1}/2)-V_{o2}+V_{o2}(d_1)=0$
$V_{o1}(1-d_2)=V_{o2}$
$V_{o2}/V_{o1}=1-d_2$ …(2)

By doing product of (1) and (2).

Figure 2: Typical Waveforms of the Proposed Converter, Including the Control Signals of the Switches, Inductors Currents, Unfiltered Step-Down Output Voltage Vab, and the Switching States for All Operating Cases: (a) Case A, (b) Case B, and (c) Case C



$(V_{o1}/V_{in})*(V_{o2}/V_{o1})=V_{o2}/V_{in}$

Voltage gain, $V_{o2}/V_{in}=(1-d_2)/(2-d_1-d_2)$ ...(3)

3.2 Case B

The voltage gains in cases B and C can also be achieved in the same way as the above procedure.

For inductor L_1,

Step-up voltage gain = $V_{o1}/V_{in}=1/(2-d_1-d_2)$ …(4)

For inductor L_2,

Step-down voltage gain = $V_{o2}/V_{in}=(1-d_2)/(2-d_1-d_2)$ …(5)

3.3 Case C

For inductor L_1,

Step-up voltage gain = $V_{o1}/V_{in}=1/(1-d2)$ …(6)

For inductor L_2,

Step-down voltage gain = $V_{o2}/V_{in}=(d_1-d_2)/(1-d_2)$ … (7)

4.0 Effect of Modulation Index on the Converter Output Voltage

Simulation of SIDO-TLC is performed in Matlab-Simulink environment. This DC-DC converter is tested for the above three cases: CaseA, CaseB & CaseC for various duty cycle. Each case is explained below. Fig. 3, Fig. 4, Fig. 5, and Fig. 6 are obtained from the Tables III, IV, and V in which the theoretical and simulation values of step-up output voltages and step-down output voltages are mentioned for 3 different cases.

4.1 Analysis of SIDO-TLC under Case A

The range of duty cycle for the converter under Case A is: ($1/2 < d_1$ and $d_2 < 1$, $d_1 > d_2$). Simulation is performed by keeping d_1=0.8 and d_2 is varied from 0.4 to 0.8.

Table III: Simulation and Theoretical Values of V_{o1} & V_{o2} by Varying d_2 and fixed D_1 under Case A with d_1=0.9

Duty Cycle	Simulation values		Theoritical values	
d_2	V_{o1} (V)	V_{o2} (V)	V_{o1} (V)	V_{o2} (V)
0.8	349.8	38.2	199.99	39.99
0.7	274.0	42.8	149.99	44.99
0.6	222.1	48.6	120.0	47.99
0.5	185.3	52.5	99.99	49.99
0.4	184.6	54.9	85.7	51.4

The dual output voltages V_{01} and V_{02} of the converter is tabulated in Table 3. V_{01} and V_{02} are calculated using (1)-(3). It is observed that V_{01} gives step-up voltage and gives step-down voltage. Variation of V_{01} with d_2 for given values of d_1 is shown in Fig. 3. It is observed that V_{01} increases with increase in duty cycles. When the graph is plotted for V_{o2} by keeping d_1 constant and varying d_2, the negative slope curve is obtained (i.e., the V_{o2} values kept on decreasing).

Figure 3: Graph for d2 Vs vo1(th)

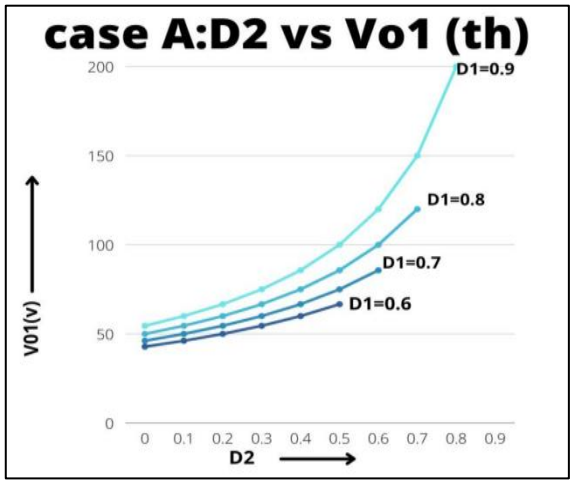
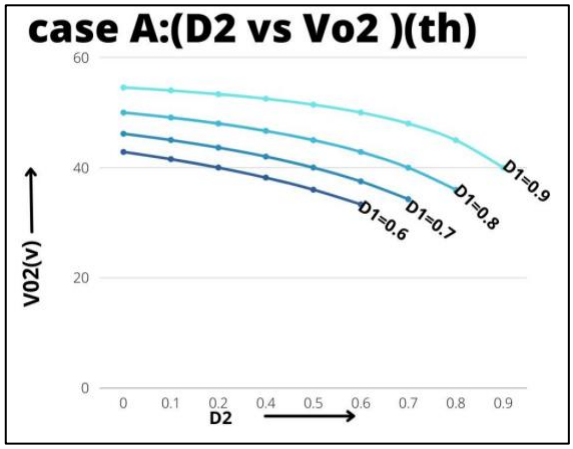


Figure 4: Graph for d_2 Vs v_{o2}(th)



4.2 Analysis of SIDO-TLC under Case B

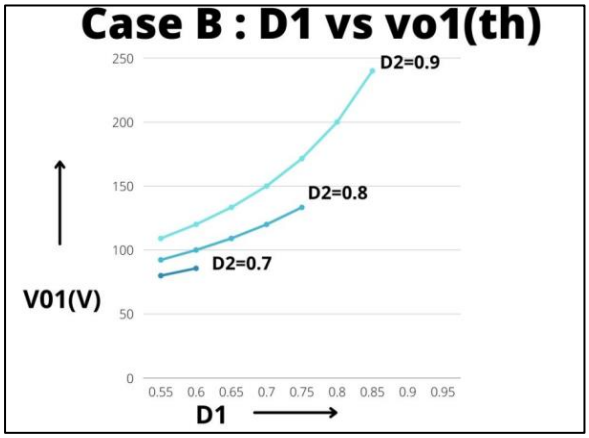
The range of duty cycle for the converter under Case B is: ($1/2 < d_1$ and $d_2 < 1$, $d_1 < d_2$). Simulation is performed by keeping d1=0.7 and d2 is varied from 0.75 to 0.95. The dual output voltages V_{01} and V_{02} of the converter is tabulated in Table 4. V_{01} and V_{02} are calculated using (4) and (5). Variation of V_{01} with d_2

for given values of d_1 is shown in Fig. 5. It is observed that V_{01} increases with increase in duty cycles.

Table 4: Simulation and Theoretical Values of V_{o1} & V_{o2} by Varying D_2 and Fixed D_1 under Case A with d_1=0.7

Duty cycle	Simulation values		Theoritical values	
d_2	V_{o1} (V)	V_{o2} (V)	V_{o1} (V)	V_{o2} (V)
0.9	220.8	4.765	120.0	12.0
0.8	190.2	8.706	100.0	20.0
0.7	167.7	15.28	85.71	25.71

Figure 5: Graph for d_1 Vs V_{o1}(th)



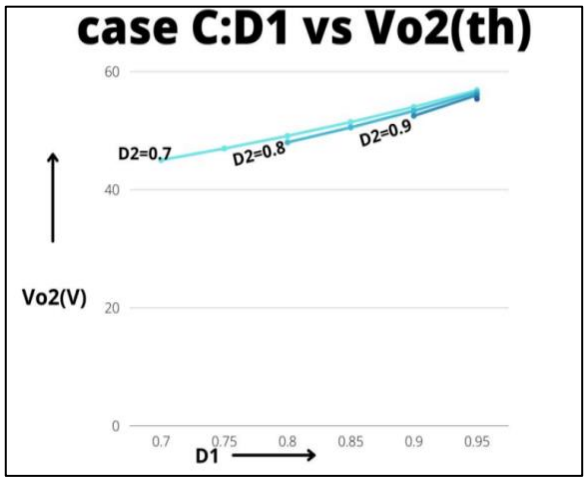
4.3 Analysis of SIDO-TLC under Case C

The range of duty cycle for the converter under Case B is: (d_2 + 1/2 < d_1 < 1, 0 < d_2 < 1/2). Simulation is performed by keeping d_2=0.2 and d_1 is varied from 0.8 to 0.95. The dual output voltages V_{01} and V_{02} of the converter is tabulated in Table V. V_{01} and V_{02} are calculated using (6) and (7). Variation of V_{02} with d_1 for given values of d_2 is shown in Fig. 6. When the graph is plotted for the V_{o2} by varying d_1 and keeping d_2 constant, the positive transient curve is obtained (i.e., the V_{o2} values kept on increasing).

Table 5: Simulation and Theoretical Values of V_{o1} & V_{o2} by Varying d_2 and Fixed d_1

Duty cycle	Simulation values		Theoritical values	
d_1	V_{o1} (V)	V_{o2} (V)	V_{o1} (V)	V_{o2} (V)
0.8	138	55.59	60	48
0.85	138	52.74	63.15	50.52
0.9	138.6	53.39	66.66	53.33
0.95	138.7	42.63	70.58	56.47

Figure 6: Graph for d1 Vs vo2(th)



5.0 Conclusion

This paper presents a high-efficiency non-isolated SIDO-TLC, whose outputs are boost and buck simultaneous. The converter is appropriate for medium- and high-voltage applications. The controllable output voltages are obtained with the help of three-level buck-boost converter. The advantages of this converter include its high efficiency, reduced passive components size and the reduced voltage stress across the semiconductor devices. The proposed converter finds its applications in electric vehicle, solar PV systems and the systems which require the multi output. This converter shows very good stability, even under simultaneous step changes of the loads and input voltage.

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