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Low-Power Design of Digital VLSI Circuits

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ABSTRACT

This paper proposes techniques like MT-CMOS, power gating, dual stack, Galeor and Lector to reduce the leakage power. A D-Flip Flop has been designed using these techniques and power dissipation is calculated and is compared with general CMOS logic of D Flip Flop. Simulation results show the validity of the proposed techniques is effective to save power dissipation and to increase the speed of operation of the circuits to a large extent.

Keywords: *Low-power design; Clock distribution; DET registers and clocking; Timing monitoring; Nanometer nodes; Dynamic clock adjustment; Multipliers; FIR filters; Memory design.*

1.0 Introduction

The word digital has made a dramatic impact on our society. The increasing prominence of portable system and the need to limit power consumption in very-high density ULSI chips have led to rapid and innovative developments in low-power design during the recent years More significant is a continuous trend towards digital solutions in all areas – from electronic instrumentation, control, data manipulation, signals processing, telecommunic ations to consumer electronics. Development of such solutions has been possible due to good digital system design and modeling techniques power losses through the methodology.

2.0 Mt-CMOS

Multi-threshold CMOS (MTCMOS) power gating is a design technique in which a power gating transistor is connected between the logic transistors and either ground, thus can creating a virtual supply rail or virtual ground rail. Gating transistor sizing, transition current, short circuit current and transition time are design issues for power gating design. as sleep transistors to reduce the leakage power from the circuit and hence consuming very less power from the source. This technique acts as a very efficient method for reducing the consumption of power. The use of power gating design results in the delay overhead in the active mode. If both nMOS and PMOS sleeptransisto are used in power gating, delay overhead will increase. This paper proposes the design methodology for reducing the delay of the logic circuits during active mode. This methodology limits the maximum value of transition current to a specified value and eliminates short circuit current. Experiment results show 16.83% reduction in the delay.

3.0 Power Gating

Power gating is a technique used in integrated circuit design to reduce power consumption, by shutting off the current to blocks of the circuit that are not in use. In addition to reducing stand-by or leakage power, power gating has the benefit of enabling Iddq testing. Operation to be seamlessly transformed into a fully DET clock gating has been fully integrated into the digital standard design flow for the first time. This is the design flow that has been proposed.

3.1 Dual-edge-triggered

Dual-edge-triggered clocking is a well-known method for reducing synchronous IC dynamic power

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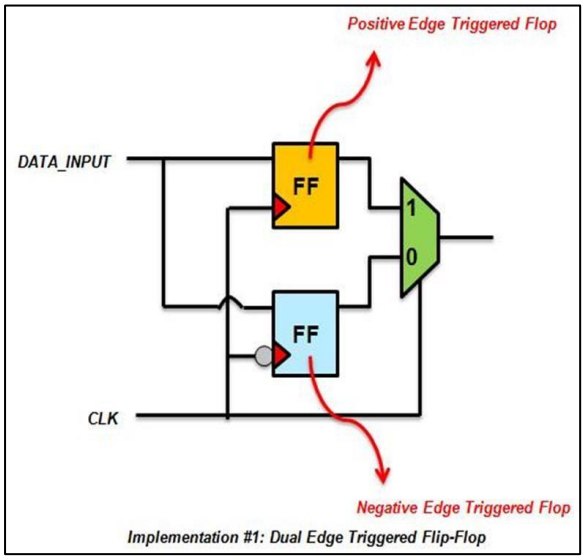
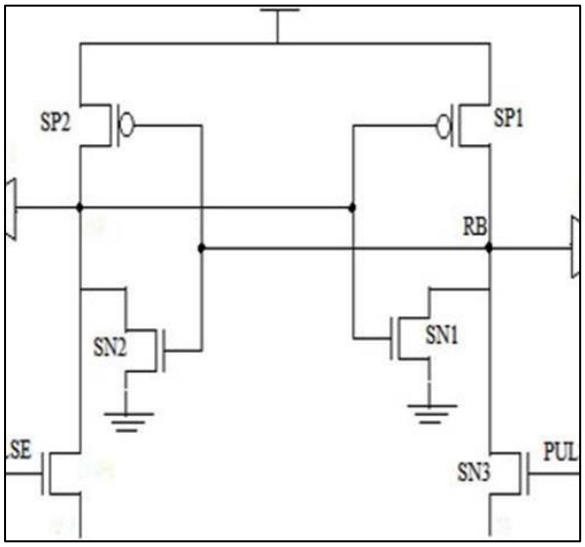
dissipation. In contrast to the traditional single-edge-triggered. In contrast to the system, which samples data on DET operation samples data on both rising and falling edges of clock, requiring half the time of the system. Dual edge triggered is frequently secondary role is used only in synchronous design, specialized uses and products. DET clocking power quickly identify the characteristics of systems.

Figure 1: Low Power Dual-Edge-Triggered





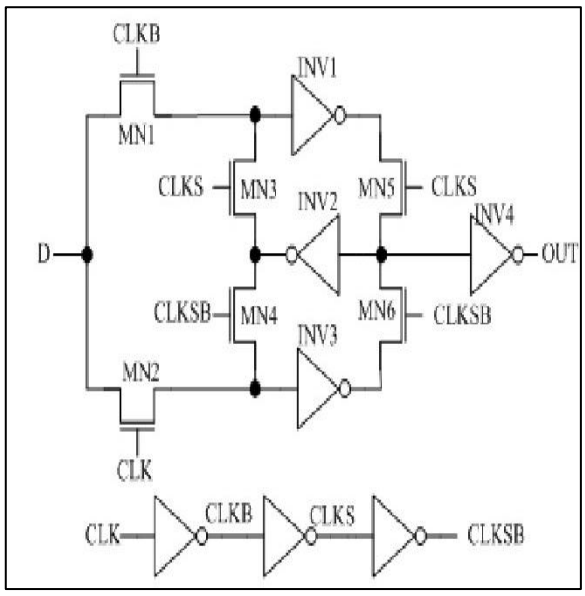
DET clocking to a conventional single-edge-triggered (SET) design in fully automated design. DET registers is proposed the flip-flop (DET-FF) that completely avoids clock-overlap. The aim of energy-quality scaling techniques small degra- dation on the QoS and lower energy consumption in digital circuits.

3.2 Proposed dual-edge triggered flip-flop

These latches are designed using one transmission gate and two inverters connected back to back and the output of both the latches are connected 2:1Mux as input. Mux is designed using one PMOS and one NMOS connected in series and gates are connected together and derived by the inverted CLK. Output of Mux is connected to the inverter for strengthening the output. back to back connected inverters hold the data when transmission gate is OFF and at the same time Mux sends the latched data to the inverter to get the correct D at the output The proposed DETFF works as follows. When the CLK is low M3, M4 and M18 are ON and M5, M6 and M17 are OFF. Hence data hold by negative latch is transparent to Q. When CLK is high M5, M6 and M17 are ON and M3, M4 and M18 are OFF.

If input D remains the same, Q also remains unchanged. On the other hand, if D is changed before the CLK then D will be hold by positive latch and the same value will be send to the output when CLK changes from Low to high and similarly for the transition of CLK from high to low.

Figure 2: Lower Power Automation DET



3.3 Automated dual edgetriggered clocking

Despite the fact that application are suitable Dual Edge Triggered Clocking, implementation of clock, as well as their integration into other systems. It is expected that the flow will be almost completely ignore. A minimum number of digital architectures

that use DET clocking have been documented. These vast majority previous papers on DET clocking have concentrated in the design ignore the complexities of DET-based system integration with electronic design automation (EDA). Furthermore, most typical cell libraries only have SET storage elements and clock-gating circuits, making it difficult to define DET restrictions for clock-tree synthesis and static timing analysis, particularly when clock- gate is used simulations are used. MC simulations are used to validate the storage cell's resilience against faults to demonstrate its durability. Second, In terms of performance and power consumption, the SDET-TSPCFF is compared. In comparison, all circuits built in a 40 nm CMOS process using standard-VT transistor. The comparison results with different DET-FFs show that the proposed SDET-TSPCFF not only solves the clock-overlap failures, but also has the lowest tcq. Because it relies heavily on tristate logic.

As a result performance is limited at near-threshold operation. The DET-latency ISLMs and power consumption are nearly identical to the DET-TGLMs, with the only difference being the output MUX Because transmission gates have lower conductivity at scaled voltage supplies, the proposed circuit has a higher tcq than the DET-TGLM.

Case Study	Number of SCs	Registers SET-SCs Area	DET-SCs Area	Area Overhead
A	228 K	18.5 % 572,009 µm2	642,505 µm2	+ 12.3 %
B	24 K	17.3 % 48,764 µm2	58,300 µm2	+ 19.55
C	37 K	9.4 % 52,245 µm2	57,953 µm2	+ 10.9 %

A circle indicates that DET power consumptions are expected to be equal. In the CS-C registers power breakdown. When all blocks are included, power is save in the clock range then power save in the registers range, owing to the DET-FFs' lower operating requency and lower power consumption when compared to their SET counterparts. Time [ns] SET implementation, due to the significant fraction of overall energy consumption of the clock tree and registers (A.7) significant total power reductions when implemented using DET clocking. The high number of registers and clock buffers result in large values of both E int and E dyn, as well as elevated activity factors Kreg and Kare, as shown in (A.7).

This is evident in mode of operation, where the DET design saves 56 percent on total power consumption, which drops to only 6 percent in the second operating mode, where clock-gating efficiency is significantly better. It's also worth noting that DET in CS-C saves a lot of power, using 58% less than the SET implementation. SET and The comparable SET frequency influences the DET/SET total power ratio. The operating points of the simulations are denoted by a cross, while the points where SET and 0.98.

3.4 Power savings

The potential for power savings is the primary reason for employing DET clocking. An accurate power analysis was performed on each of the three test blocks.

The resultant power numbers show the power consumption for both clocking systems. For each case study, the simulated clock frequency in the DET design is half of the SET clock frequency to provide similar throughput in both implementations. The consumption of power are divide into register and combinatorial logic, as well as a total power usage summary. To lay the groundwork for a more in-depth investigation, each bar in the plot is further divide into internal power, switching power, and leakage power.

4.0 Conclusions

In this Paper, analysis of sequential circuit (D This part illustrated potential of Failure due to overlapping of clock in which DET-FFs use transmission gates as output MUX, exhibiting without rate of error at Vth is 40 nm in CMOS technology. In this area static TSPC Dual edge triggered flip flop eliminates the overlapping the clock changes, and across temperature. Furthermore, among popular DET-FF registers, the register provide power-delay product and CK-to-Q delay.

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